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# Design Considerations for 48V-VRM: Architecture, Magnetics, and Performance Tradeoffs


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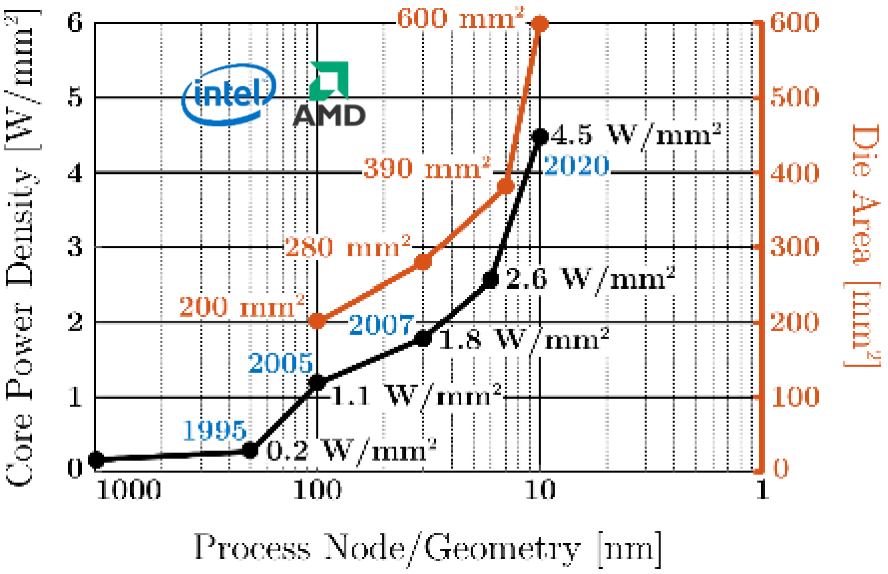
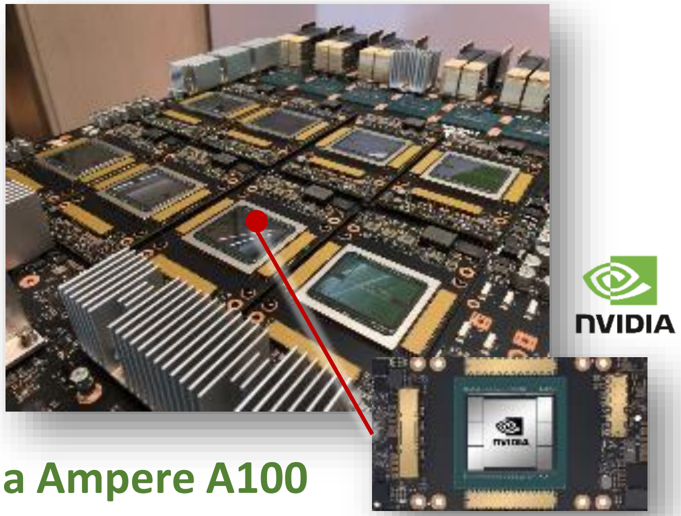
# Massive Power Demand for Future Computing

- Transistor density is rapidly growing
- Processor die area is continuously expanding
- More microprocessors on server motherboards

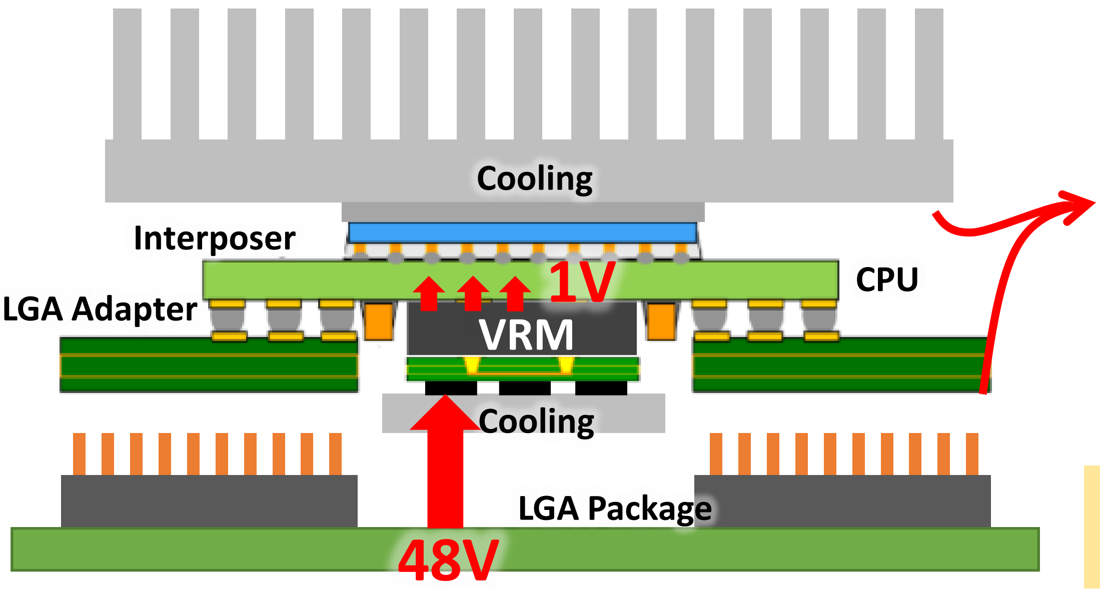
- *J. Beak, M. Chen et al., "Vertical Stacked LEGO-PoL CPU Voltage Regulator," TPEL'22.*

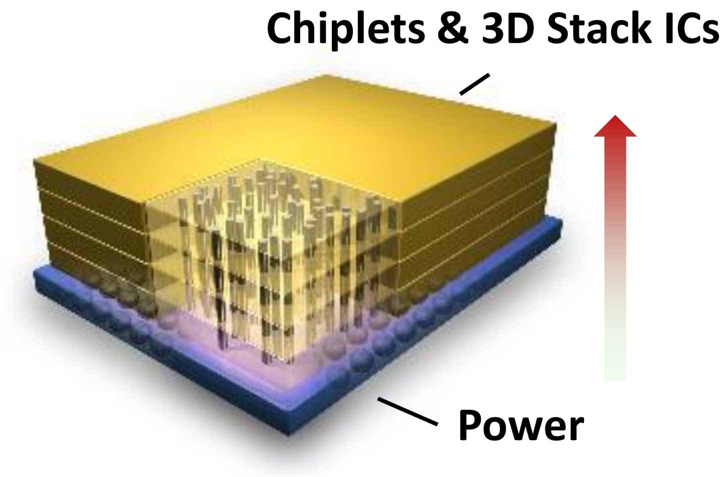


**Nvidia Ampere A100**
**48V-1V, 1000A**

# Vertical Power Delivery to Chiplets and 3D-ICs




*More Power → Higher $V_{IN}$ (96V?)*
*Better Computing → Lower $V_{OUT}$ (0.5V?)*

| Example Specs: | 48V-1V | >1A/mm² | <7 mm height | 500A~1000A | 5A/ns | 90% |
|---|---|---|---|---|---|---|
| | *Conversion Ratio* | *Area Density* | *Power/Signal/Thermal* | *Transient* | *Efficiency* | |

# 48V VRM Key Milestones since 2012

12V VRM | 48V VRM

**2012**

**Legacy 2-stage solution:**
1st stage isolated & regulated 48V-12V, leveraged from legacy telecom industry.

**1-stage solution:**
Vicor 48V-PoL direct conversion

**2016**

**Google 48V architecture**

STMicro, Maxim, TI 48V-PoL direct conversion solutions released

Google 48V STC based 2-stage architecture disclosed at APEC 2017

**2018**

**Nvidia 48V GPU (DGX-2, 10kW)**

**48V 2-stage ecosystem from Google through OCP:**
1. 1st stage 48V-12V (fixed ratio & regulated hybrid converters);
Available solutions from ST, Maxim, ADI, Renesas, Infineon, Vicor,...
2. 2nd stage multiphase buck.

**Power Stamp Alliance**
**ST, ADI, TI, MPS, Infineon**
**48V VRM products released**

**2020**

**48V 2-stage architecture further evolved:**
1. 1st stage 48V-bus (12V or lower, fixed ratio & regulated hybrid converters);
2. 2nd stage multiphase TLVR adopted by mainstream servers for fast transients.

**2022**

**Intel PowerVia**
**Tesla Dojo**
**Nvidia H100**

**High density, high efficiency, high bandwidth, 2.5D/3D vertical power delivery**

**Apple M1 (coupled magnetics)**

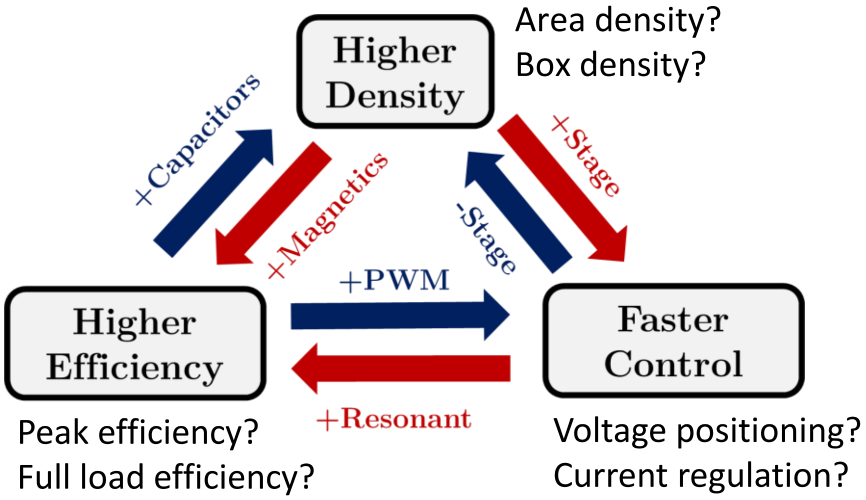
*Credit: Shuai Jiang, Google*

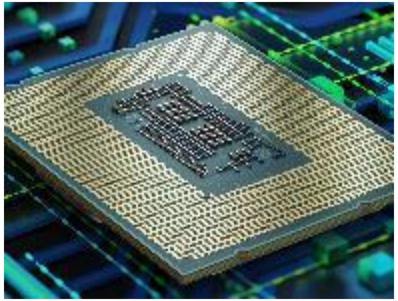
CPES · Georgia Tech · Berkeley, University of California · Princeton University · UC San Diego · Dartmouth · UT Dallas

# Architecture Considerations for 48-V VRM

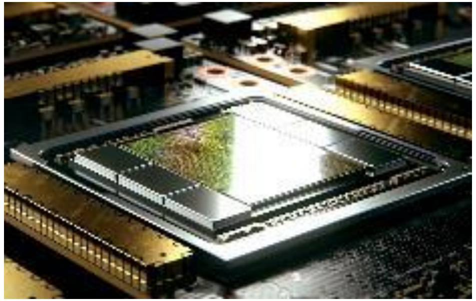


1. Number of Stages: Single-Stage / Multi-Stage?
2. Passive Component: Capacitor-based / Inductor-based / Transformer-based?
3. Operation Mechanism: Resonant / PWM?
4. Regulation Mechanism: Current Source / Voltage Source?



**Intel CPUs**

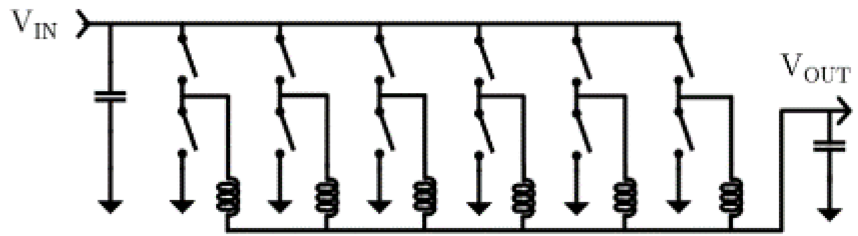


**Nvidia GPUs**

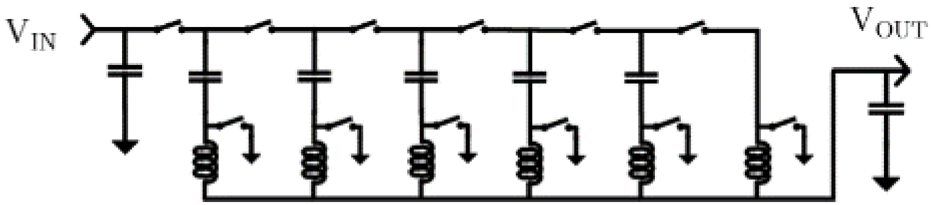
*Co-Design Opportunities*

*Hardware / Software / Power / Packaging / Thermal / Signal*

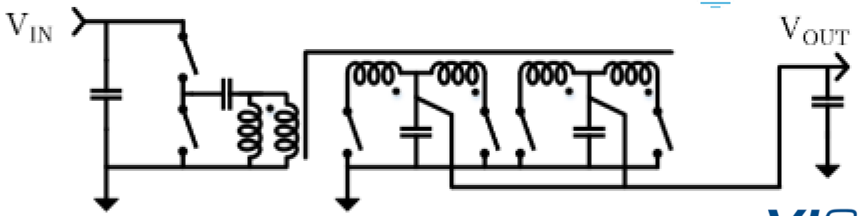
# Single-Stage Power Architecture



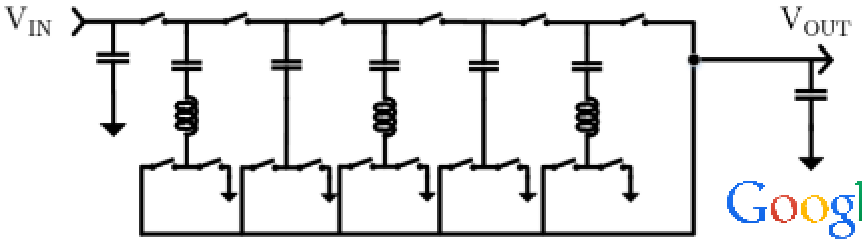

(a) Multiphase Buck / PWM




(c) Hybrid Switched-Capacitor PWM




(b) Transformer-based Resonant / PWM




(d) Hybrid Switched-Capacitor Resonant


- X. Zhou, P.-L. Wong, P. Xu, F. Lee, and A. Huang, “Investigation of candidate vrm topologies for future microprocessors,” TPEL’20.
- K. Nishijima, K. Harada, T. Nakano, T. Nabeshima, and T. Sato, “Analysis of double step-down two-phase buck converter for vrm,” INTELEC’05.
- M. H. Ahmed, C. Fei, F. C. Lee, and Q. Li, “48-v voltage regulator module with pcb winding matrix transformer for future data centers,” ITIE’17.
- S. Jiang, S. Saggini, C. Nan, X. Li, C. Chung, and M. Yazdani, “Switched tank converters,” TPEL’19.


- *High efficiency*
- *Low component count*
- *Challenges in control*

# Multi-Stage Power Architecture

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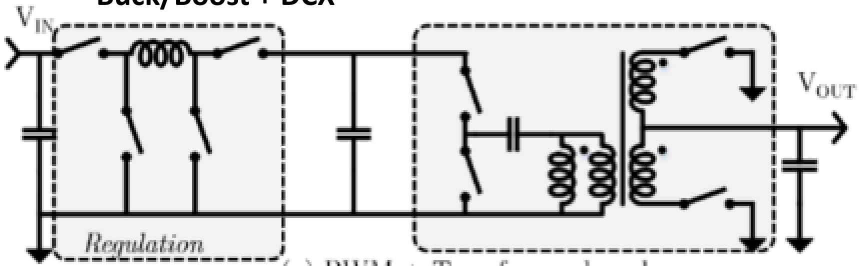
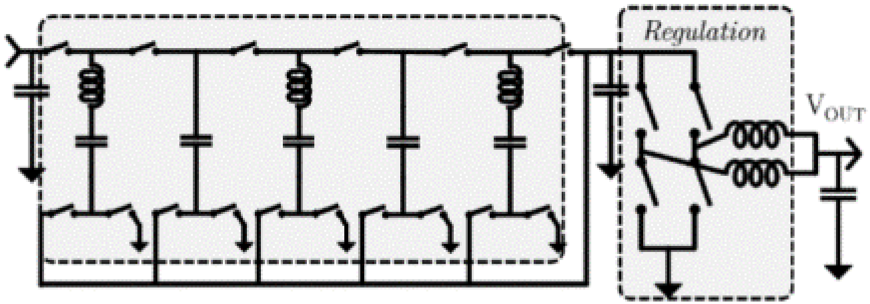
**Buck/Boost + DCX**




(a) PWM + Transformer-based

VICOR

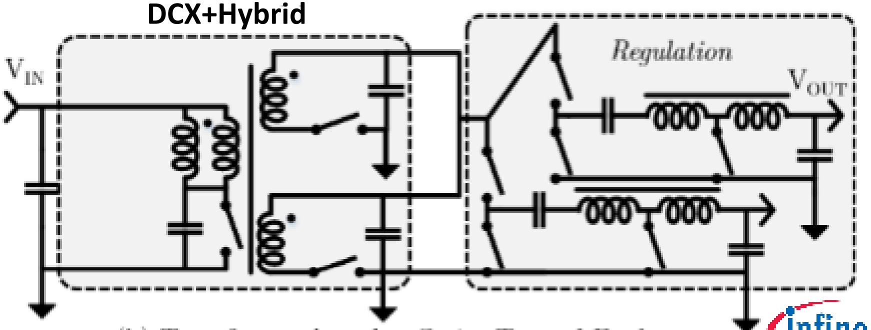
**DCX+Buck**




(c) Switch-Tank + Buck

Google

**DCX+Hybrid**



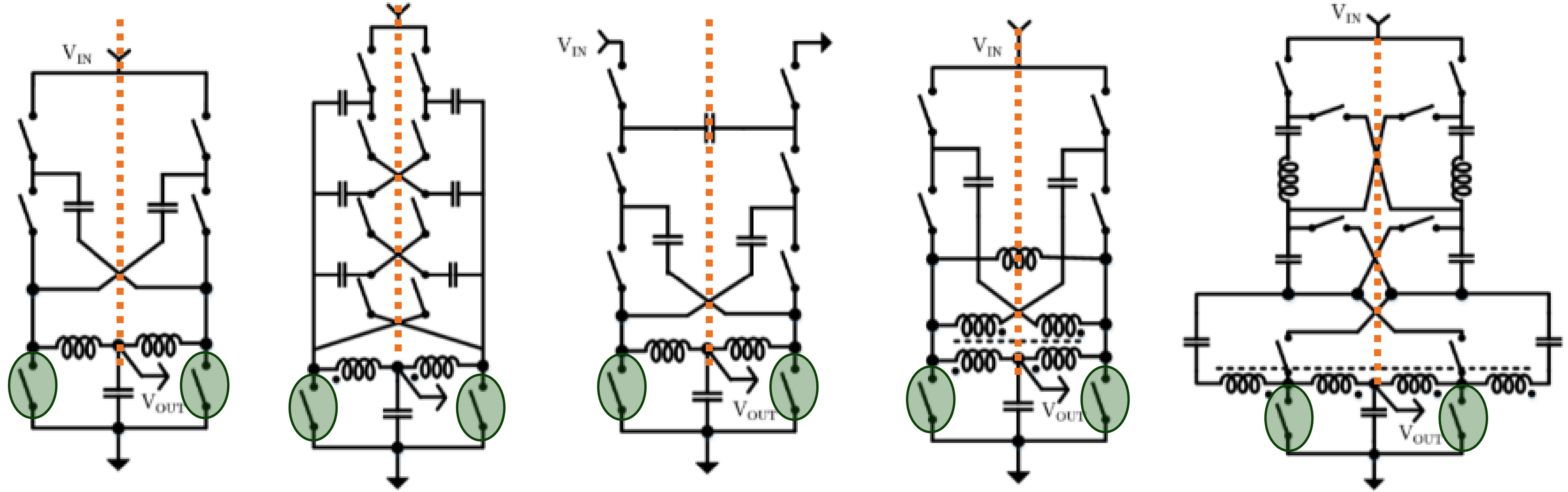

(b) Transformer-based + Series Tapped Buck

infineon

**Intermediate Bus : 24V, 12V, 8V, 6V, 4V, …**


- "Vicor Power-on-Package: Redefining 48V to PoL regulation for high-power processors and AI ASICs." [Online]. Available: https://www.vicorpower.com/industries-and-innovations/power-on-packageseeitinaction
- J. A. Cobos, A. Castro, Garć ıa-Lorenz, J. Cruz, and Cobos, "Direct power converter -dpx- for high gain and high current applications," in 2022 IEEE Applied Power Electronics Conference and Exposition (APEC), 2022, pp. 1016–1022.
- M. Chen, P. S. Shenoy, and J. Morroni, "A series-capacitor tapped buck (sc-tab) converter for regulated high voltage conversion ratio dc-dc applications," IEEE Energy Conversion Congress and Exposition (ECCE), 2014, pp. 3650–3657.
- M. Ursino, S. Saggini, S. Jiang, and C. Nan, "High density 48v-to-pol vrm with hybrid pre-regulator and fixed-ratio buck," in Applied Power Electronics Conference and Exposition, 2020, pp. 498–505.

# Single-Stage Hybrid Switched-Capacitor Converters




(a) Stacked Series-Buck

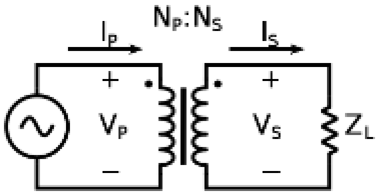
(b) Hybrid-Dickson

(c) Quadruple Step-Down Buck (Hybrid FCML+Buck)

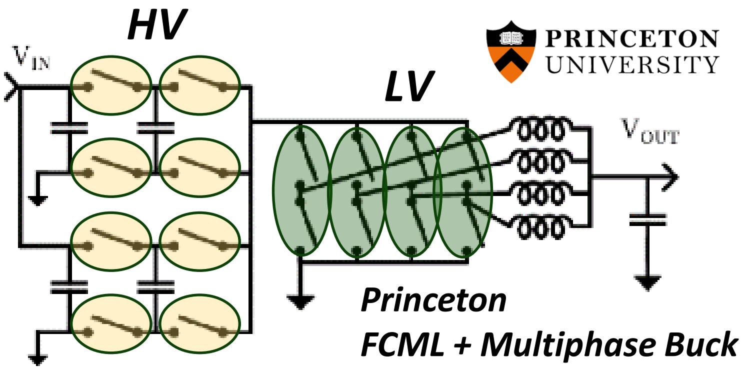
(d) LLC + SC

(e) Stacked LLC + ReSC (Multi-Resonant Hybrid SC)

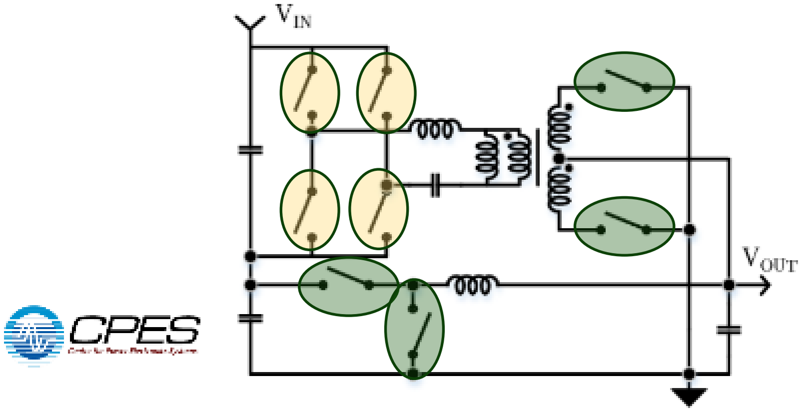
- *Series stacked switches and capacitors to step the voltage down*
- *Unbalanced voltage and current stress in top and bottom switches*
- *Transformers naturally provides voltage/current stress balancing*



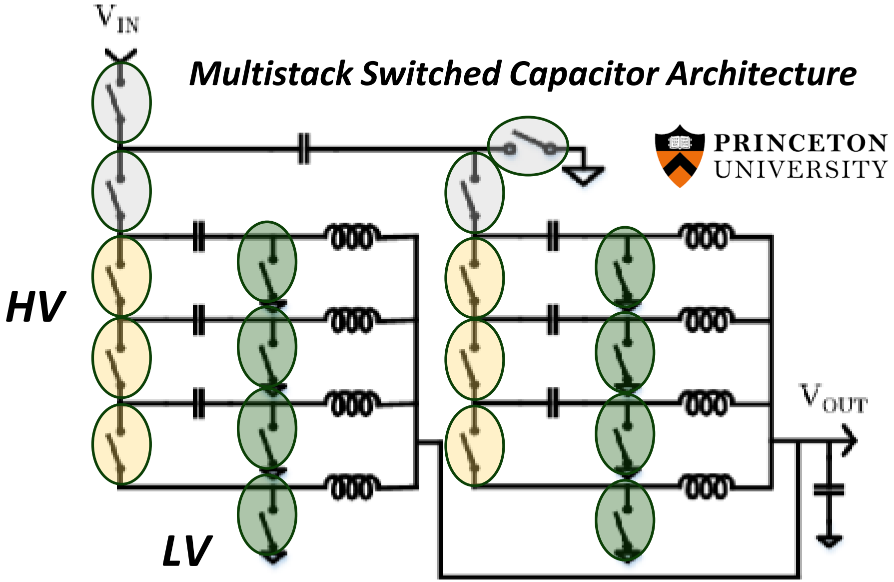
# Hybrid Architecture with Granular Cells




Princeton
FCML + Multiphase Buck




CPES Sigma: Transformer DCX + Stacked Buck

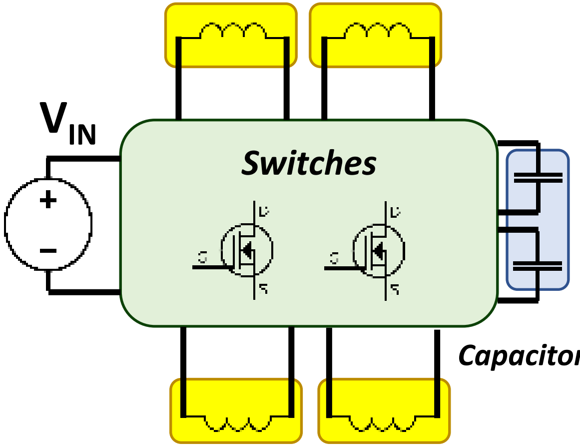




- Y. Chen, P. Wang, H. Cheng, G. Szczeszynski, S. Allen, D. M. Giuliano, and M. Chen, “Virtual intermediate bus cpu voltage regulator,” TPEL’22.
- P. Wang, D. Zhou, D. Giuliano, M. Chen and Y. Chen, "Multistack Switched-Capacitor Architecture with Coupled Magnetics for 48V-to-1V VRM," COMPEL’22.
- G. Roberts, N. Vukadinoví c, and A. Prodic, “A multi-level, multi-phase buck converter with shared flying capacitor for vrm applications,” APEC’18.
- M. H. Ahmed, C. Fei, F. C. Lee, and Q. Li, “Single-stage high-efficiency 48/1 v sigma converter with integrated magnetics,” IEEE Trans. on Ind. Electron., vol. 67, no. 1, pp. 192–202, 2020.

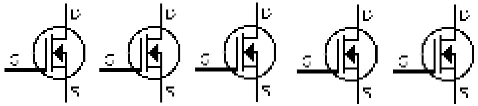
# Principles of Granular Power Conversion

*Traditional*

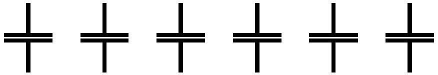



*Building Blocks*

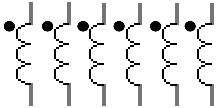
Granular Switches



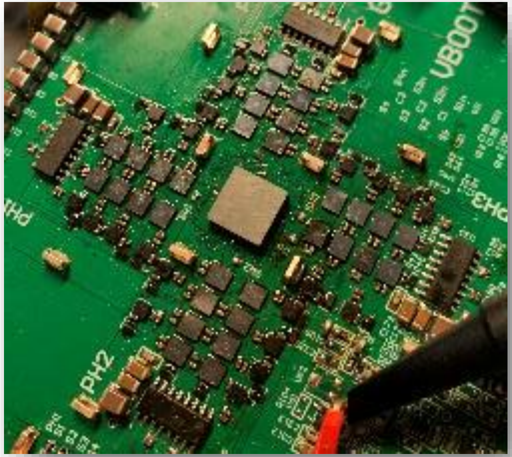
Granular Capacitors



Integrated Magnetics



*Distributed SwCap + Integrated Magnetics*

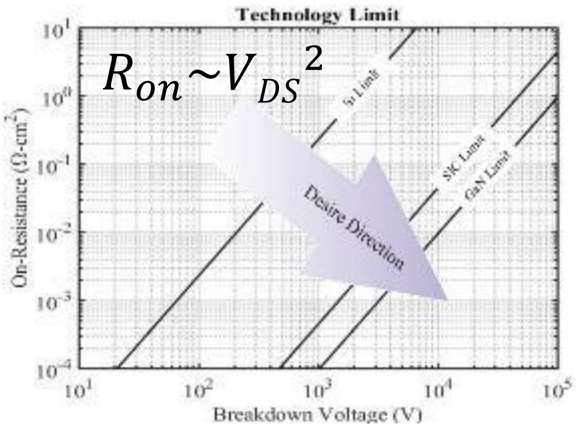


*Smaller, More Efficient, Faster, New Functions*

1. ***Why granular power conversion? Which application?***
2. ***Design methods to maximize the advantages of granular power conversion?***

# Scaling Laws of Granular Power Electronics Components

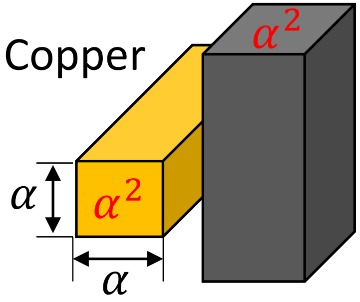
- **Switches (R)**




"Baliga Figure-of-Merit"

*Smaller switches better*

- **Magnetics (L)**



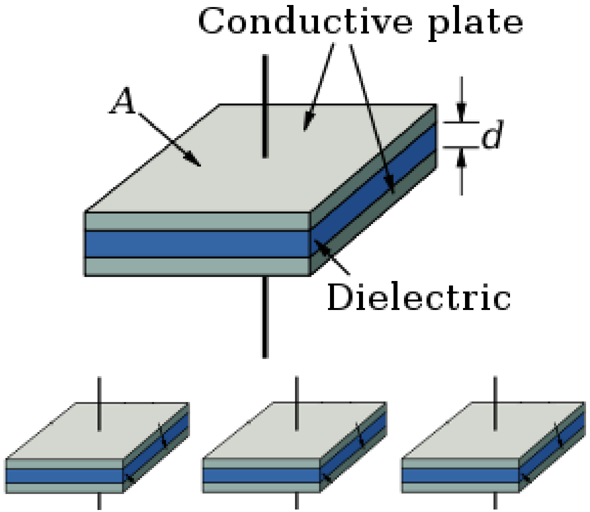

Copper Area ~ $I$ ~ $\alpha^2$

Ferrite Area ~ $V$ ~ $\alpha^2$

Power / Volume ~ $\alpha^{4/3}$

*Larger magnetics better*

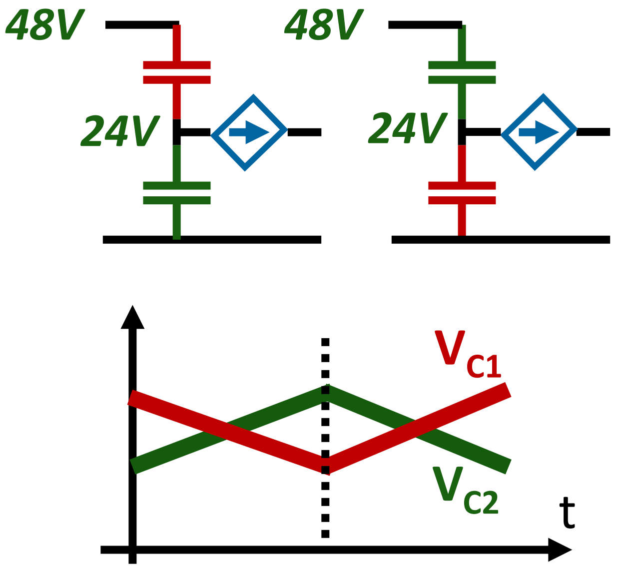
- **Capacitors (C)**

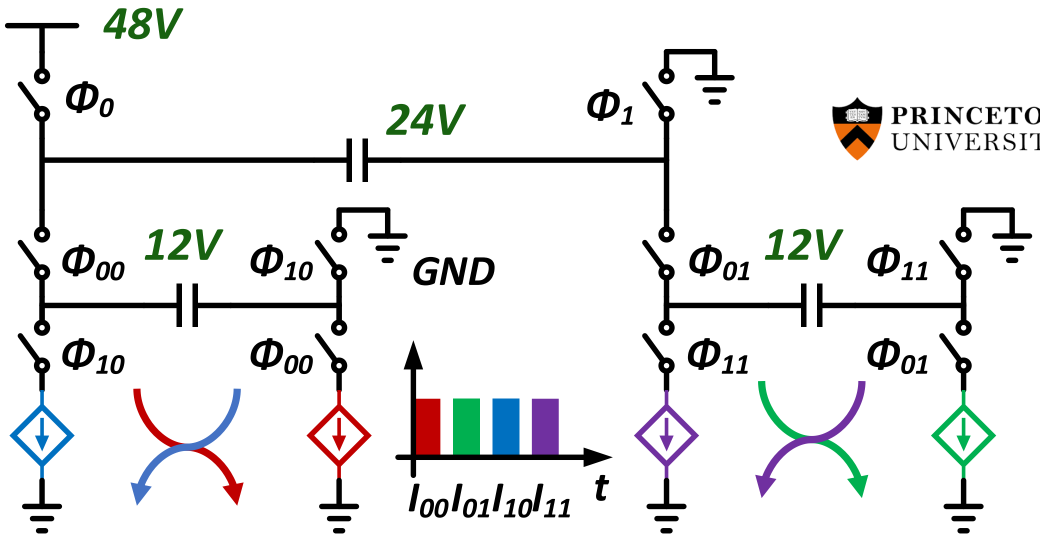



*Capacitors - indifferent*


- *B. J. Baliga, Fundamentals of Power Semiconductor Devices, ISBN-13: 978-0387473130, 1996.*
- *S. Ćuk, "A New Zero-Ripple Switching DC-to-DC Converter and Integrated Magnetics," IEEE Transactions on Magnetics, March 1983.*
- *C. R. Sullivan et al., "On size and magnetics: Why small efficient power inductors are rare," 3D-PEIM'16.*

# Soft-Charging for Hybrid Switched-Cap Circuits

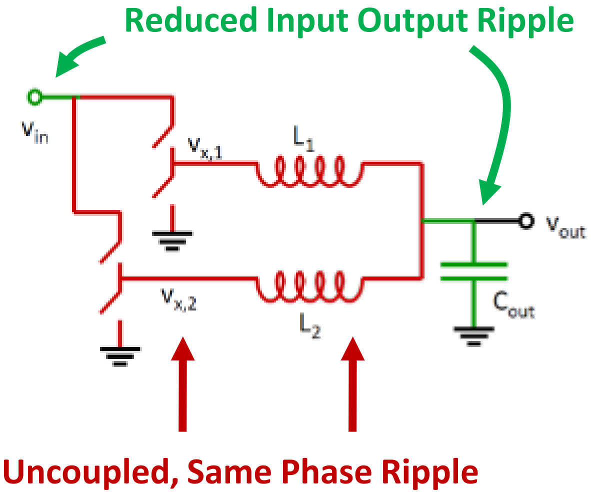


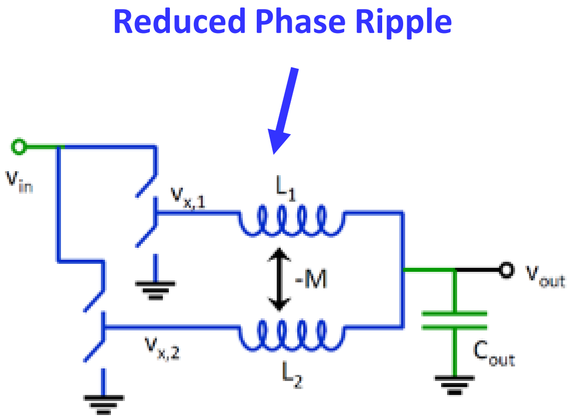



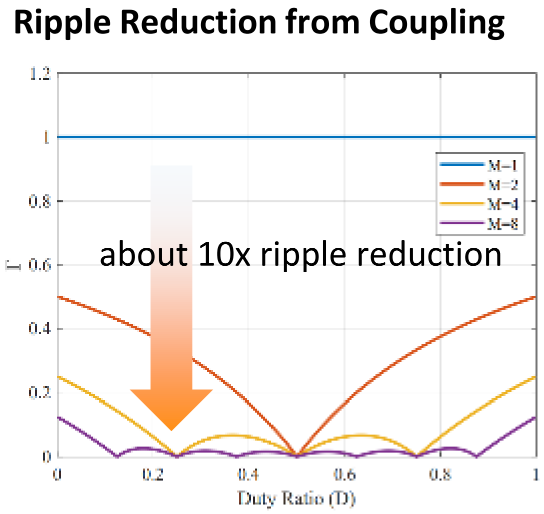


- *D. M. Giuliano, M. E. D'Asaro, J. Zwart, and D. J. Perreault, "Miniaturized low-voltage power converters with fast dynamic response," IEEE Trans. Emerg. Sel. Topics Power Electron., vol. 2, no. 3, pp. 395–405, Sep. 2014.*
- *R. C. N. Pilawa-Podgurski, D. M. Giuliano, and D. J. Perreault, "Merged-two-stage power converter architecture with soft charging switched capacitor energy transfer," in Proc. IEEE Power Electron. Specialists Conf., Rhodes, Greece, 2008, pp. 4008–4015.*
- *M. Chen, Merged Multi-Stage Power Conversion: A Hybrid Switched-Capacitor Magnetics Approach, Ph.D. Thesis, MIT, June 2015.*

# Unified Models for Multiphase Coupled Inductors




- Interleaving Ripple Reduction Ratio

$$\Gamma = \frac{(k+1-DM)(DM-k)}{(1-D)DM^2}$$

- Magnetic Coupling

$$\beta = \frac{MR_C}{R_L}$$

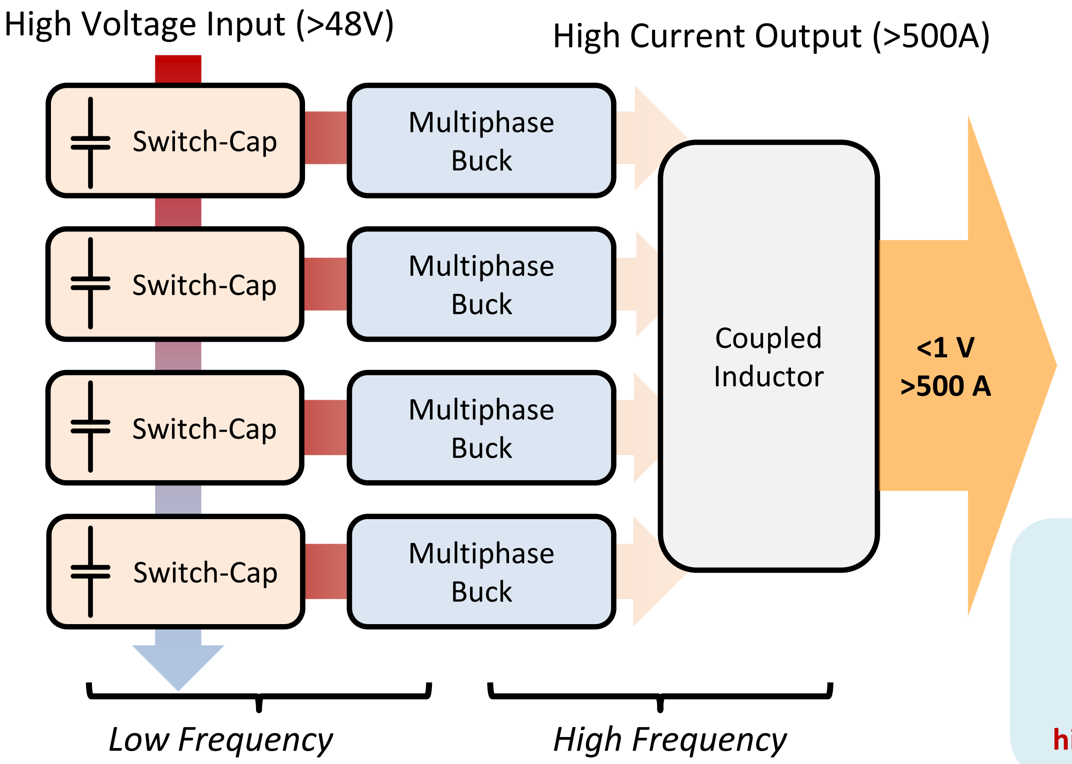
- Coupling Ripple Reduction Ratio

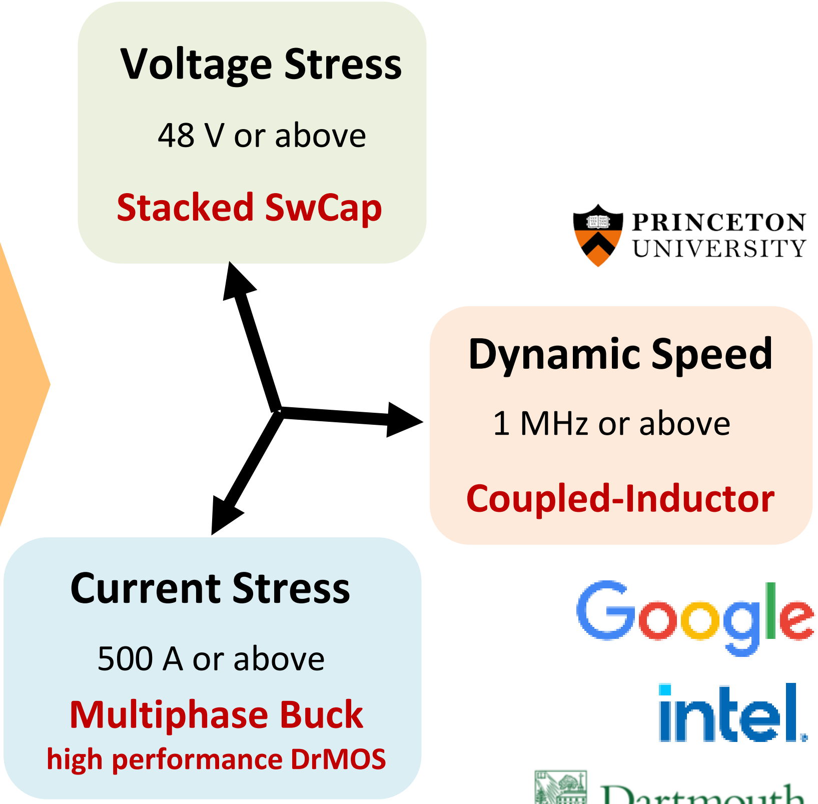
$$\gamma = \frac{1+\beta\Gamma}{1+\beta}$$

- Stronger coupling → better ripple reduction and faster dynamics

- *M. Chen and C. R. Sullivan, "Unified Models for Coupled Inductors Applied to Multiphase PWM Converters,"* ***TPEL'21 Prize Paper***.

# Princeton Granular LEGO Point-of-Load Architecture




- *J. Beak et al., "Vertical Stacked LEGO-PoL CPU Voltage Regulator," TPEL'22.*

# Automatic Voltage Balancing and Current Sharing

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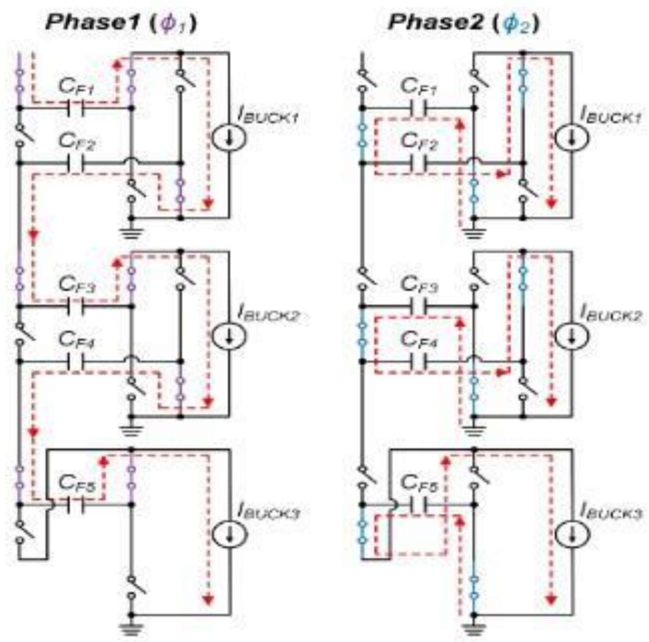
## ➢ Automatic Current Sharing

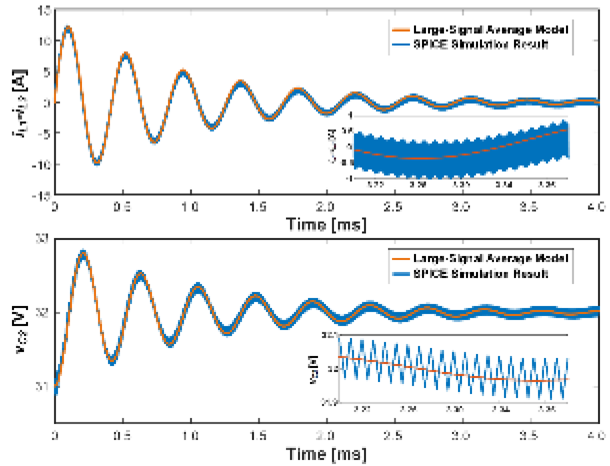



## ➢ Dynamics of Switched Capacitor Voltages

$$\ddot{X} + \frac{R}{L}\dot{X} + \frac{D^2}{4LC} M X = 0,$$

$$\ddot{X} = \begin{bmatrix} \frac{d^2 i_{L1}}{dt^2} \\ \frac{d^2 i_{L2}}{dt^2} \\ \vdots \\ \frac{d^2 i_{LN}}{dt^2} \end{bmatrix}, \quad \dot{X} = \begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \vdots \\ \frac{di_{LN}}{dt} \end{bmatrix}, \quad X = \begin{bmatrix} i_{L1} \\ i_{L2} \\ \vdots \\ i_{LN} \end{bmatrix},$$

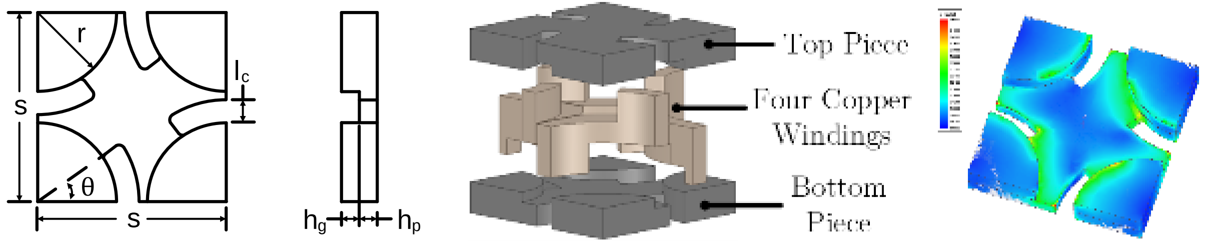
$$M = \begin{bmatrix} 1 & -1 & 0 & 0 & \cdots & 0 \\ -1 & 2 & -1 & 0 & \cdots & 0 \\ 0 & -1 & 2 & -1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \cdots & \vdots \\ 0 & 0 & \cdots & -1 & 2 & -1 \\ 0 & 0 & \cdots & 0 & -1 & 1 \end{bmatrix}.$$

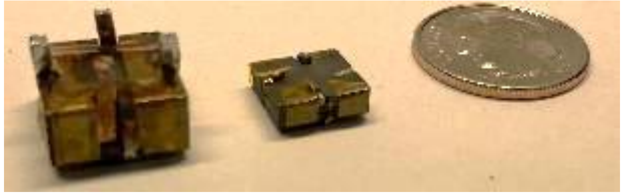



- Inductors soft-charge the switched capacitors
- Automatic current balancing of switched-capacitor circuits
- Low frequency step down & high frequency regulation

- *J. Beak et al., "Vertical Stacked LEGO-PoL CPU Voltage Regulator," TPEL'22.*

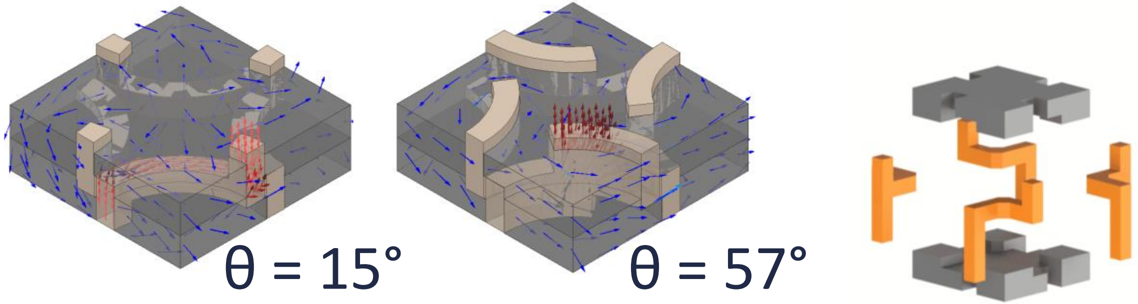
# Mini-LEGO: Vertical Coupled Inductor Structures



**Parameter for geometry design: s, r, lc, θ, h**

**Winding wrap around core** **Core wrap around winding**



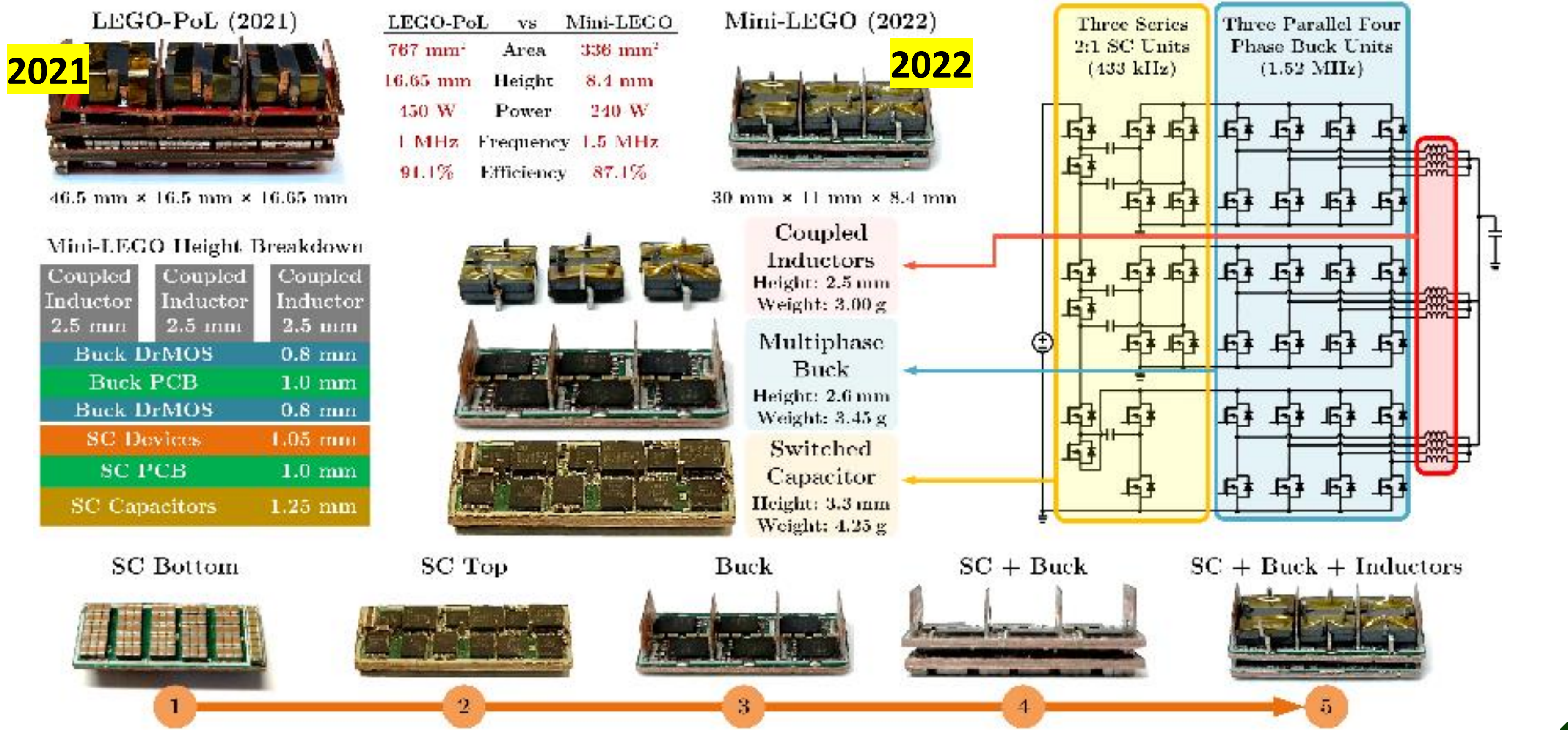

| Version 1 Magnetics (1 MHz) | Version 2 Magnetics (2 MHz) | US Dime |
|---|---|---|
| 12 x 12 x 5 $mm^3$ | 8 x 8 x 3 $mm^3$ | |

25 A per phase 100 A per $cm^2$

- *J. Beak et al., "Vertical Stacked LEGO-PoL CPU Voltage Regulator," TPEL'22.*

# From LEGO-PoL to Mini-LEGO - 2x density in 18 Months



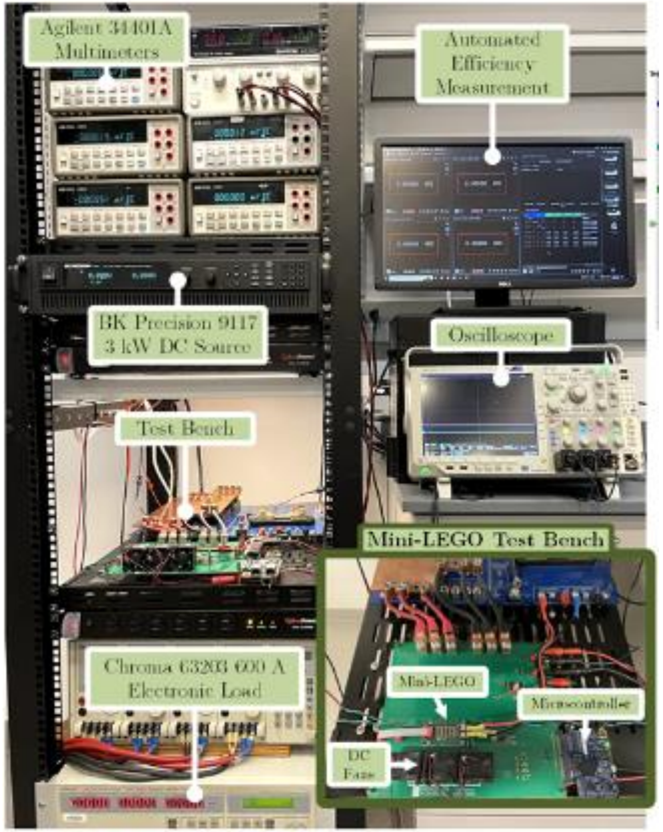



| LEGO-PoL | vs | Mini-LEGO |
|---|---|---|
| 767 mm² | Area | 336 mm² |
| 16.65 mm | Height | 8.4 mm |
| 150 W | Power | 240 W |
| 1 MHz | Frequency | 1.5 MHz |
| 91.1% | Efficiency | 87.1% |

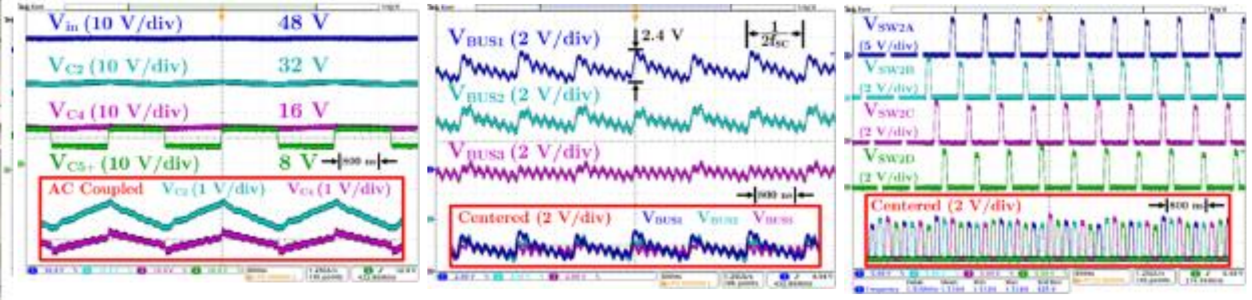
Mini-LEGO Height Breakdown

| | | |
|---|---|---|
| Coupled Inductor 2.5 mm | Coupled Inductor 2.5 mm | Coupled Inductor 2.5 mm |
| Buck DrMOS | | 0.8 mm |
| Buck PCB | | 1.0 mm |
| Buck DrMOS | | 0.8 mm |
| SC Devices | | 1.05 mm |
| SC PCB | | 1.0 mm |
| SC Capacitors | | 1.25 mm |

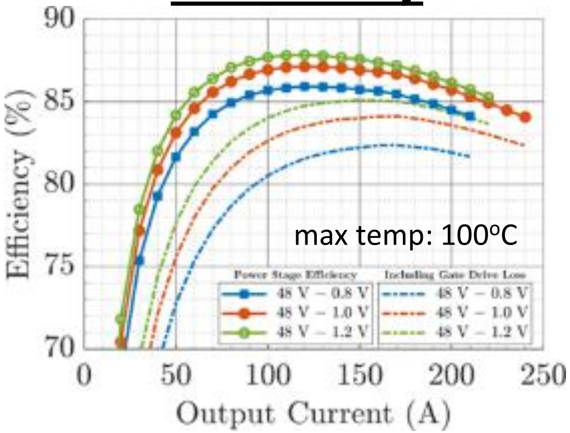
# Mini-LEGO: Experimental Results




## Steady-State Waveforms (1 V / 240 A)




## Efficiency



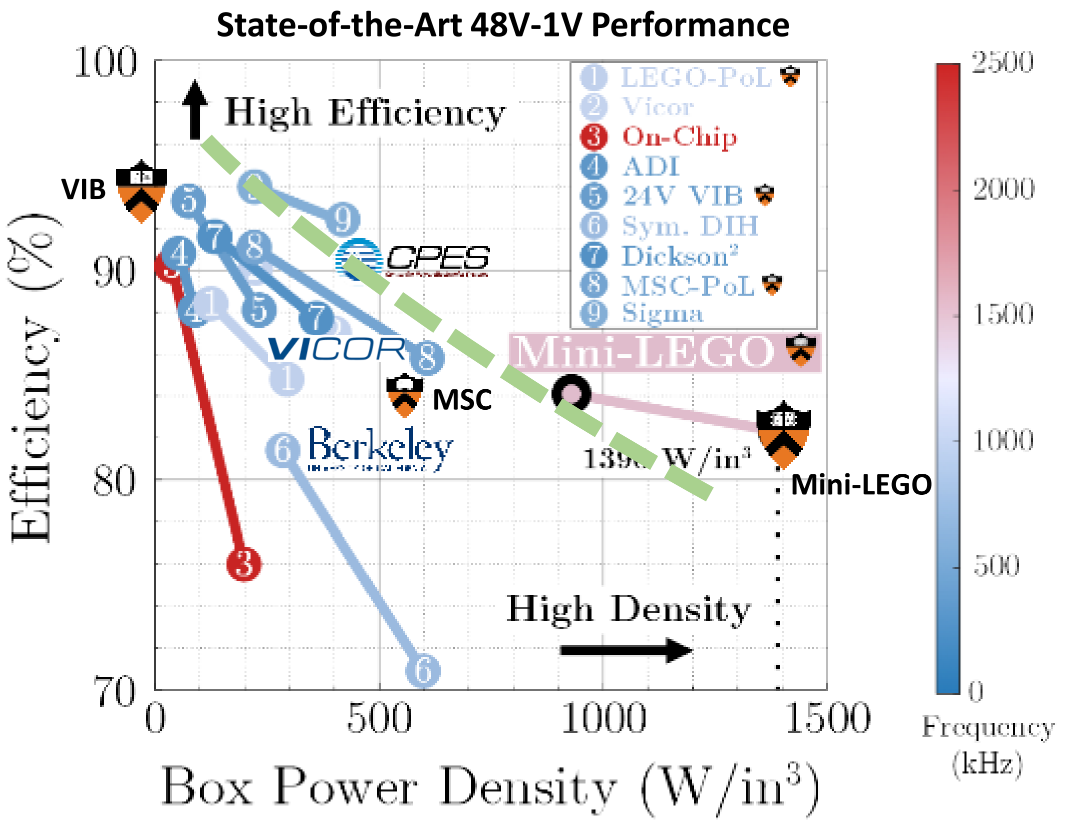

87.1% Peak Efficiency at 1 V / 120 A

*84.1% including gate drive losses*

84.1% Full Load Efficiency at 1 V / 240 A

*82.3% including gate drive losses*

# State-of-the-Art 48V VRM Designs




## Mini-LEGO

**Current Area Density**

0.71 A/mm$^2$

**Power Density**

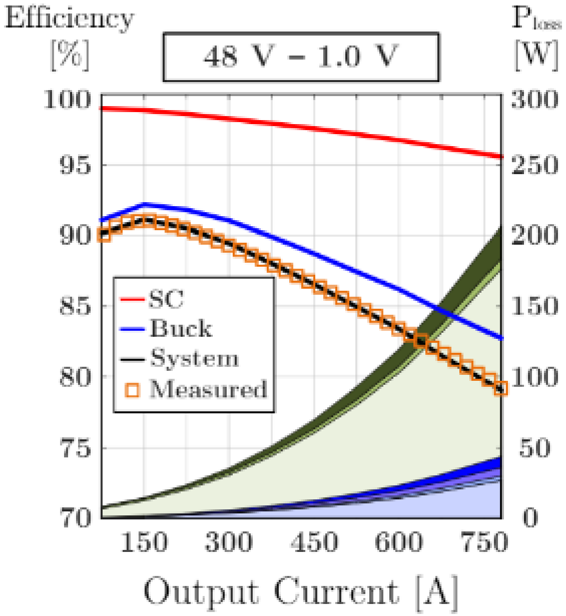
1390 W/in$^3$

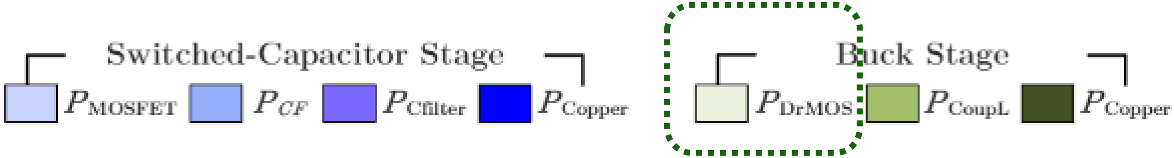
**Switching Frequency**

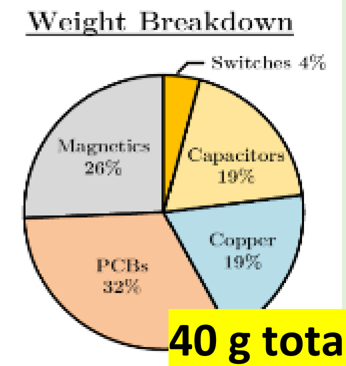
1.52 MHz

* All designs are presented with gate drive loss and size included, for 48 V to 1 V conversion

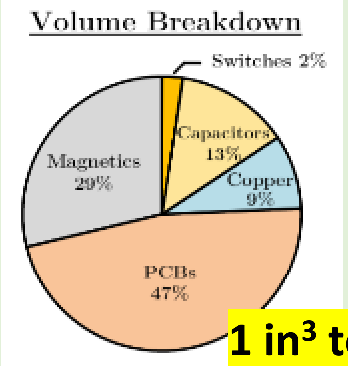
# Loss Analysis and Performance Evaluation



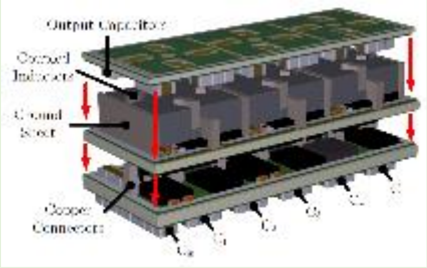




**40 g total**




**1 in$^3$ total**



***Mini-LEGO***

***$R_{dson}$ is still the bottleneck***

***Acknowledgement***

Google
Infineon
intel
Semiconductor Research Corporation
tsmc
pSemi