

# Machine-Learning-Based Optimization: The Future of Power Package Design

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Collaborative research with Prof. Madhavan Swaminathan, Prof. Yogendra Joshi  
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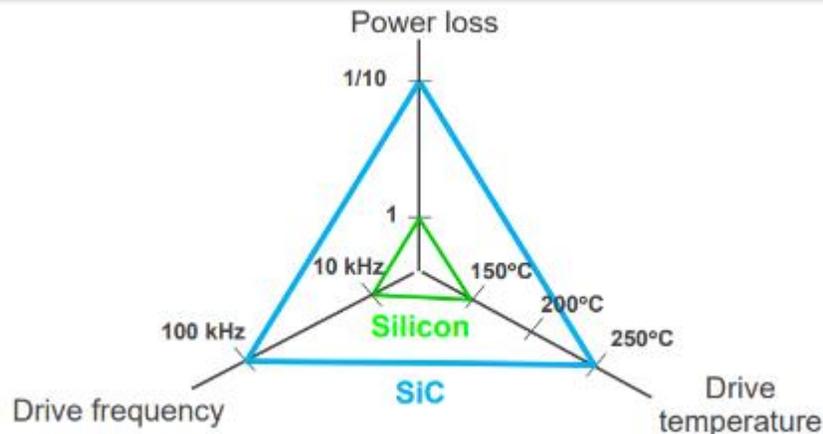
- **Background**
  - Need for Advanced Packaging for SiC-Based Heterogeneously-Integrated Motor Drives
- **Technical Approach**
  - Automation of Design and Optimization
  - Benchmarking vs. Existing EDA Tools
- **Workflow**
  - Creation of Power Module
  - Visualization Optimization Results
  - Post-Optimization Analysis
  - Designs
- **Example Applications**
- **Summary & Considerations for Future EDA Tools**

## Modern EV Usage



- Need for flexible & scalable electric systems with increased mileage

## The Promise of SiC

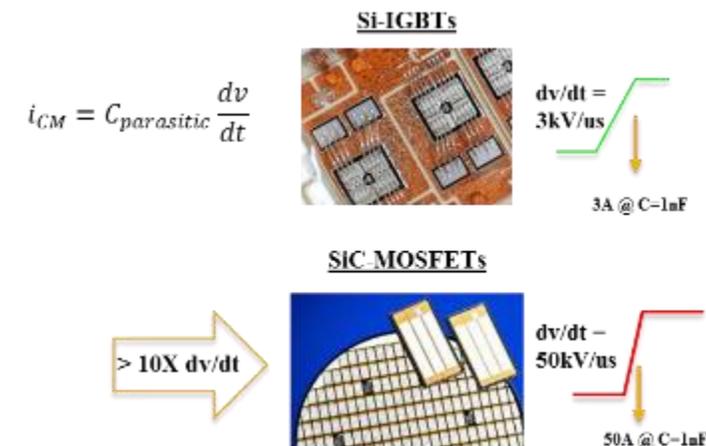


B. K. Chakravarthy et al., E3S Web Conf., 2019.

- Smaller die sizes
- Lighter passives
- Reduced cooling requirements

➤ 5X smaller traction inverters

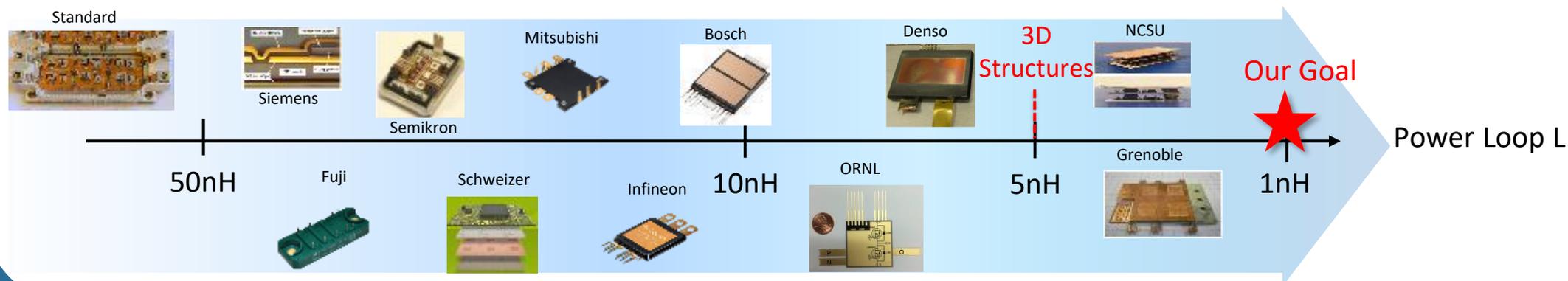
## Why it's not really happening



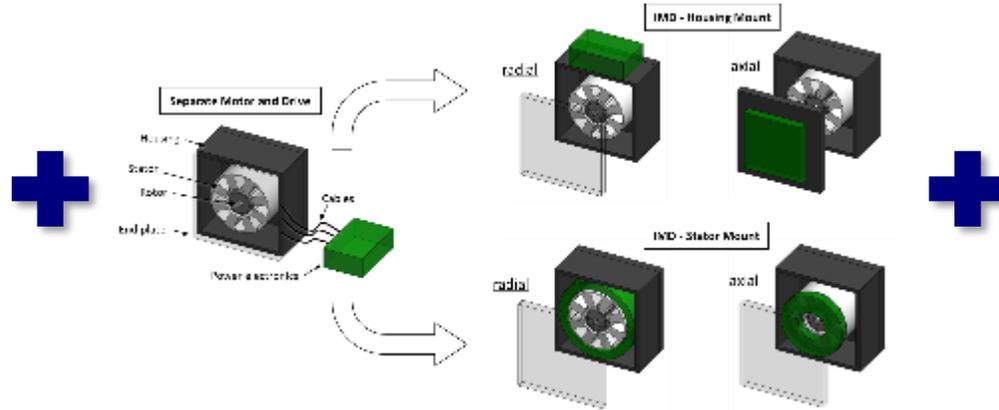
- Chip-package interactions with parasitic L,C – increased di/dt & dv/dt
- Lack of high-temp. packaging
- Thermal densification & near-junction cooling integration

- Traditional packaging solutions developed for Si technology – now limiting benefits of SiC
- Co-integration of power electronics, motor and cooling – complex, system-level perspective

Metrics	Prior Art	Research Focus
Power Density	< 100 kW/L	> 300 kW/L
Parasitic Inductance	5 – 52 nH	< 1 nH
Parasitic Capacitance	75 – 140 pF	< 0.1 pF
Heat Flux	< 1 kW/cm <sup>2</sup>	> 1 kW/cm <sup>2</sup>
Max. Junction Temperature	< 175°C	> 200°C
Junction-to-Coolant R <sub>th</sub>	0.1 – 1.1°C/W	> 20% reduction
Thermal Performance	Steady-state only	Thermal Transient Suppression
Breakdown Voltage	< 30 kV	> 30 kV
Reliability	Power & Thermal Cycling	At increased T <sub>jmax</sub> & ΔT
Integration	Inverter box, separate cooling loops	Integrated motor drive

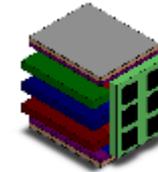


## Today's Traction Inverter



## Our Vision

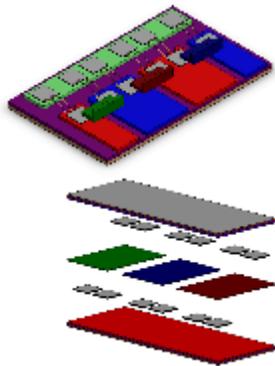
3D "stacked" module with substrate-integrated cooling



- Disruptive rather than incremental path to performance & reliability
- Multi-level 3D architectures
- Heterogeneous, multi-functional integration
- ML-based multi-physics co-design

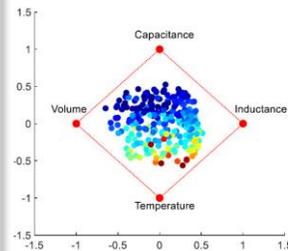
## Research Focus Area

### Design



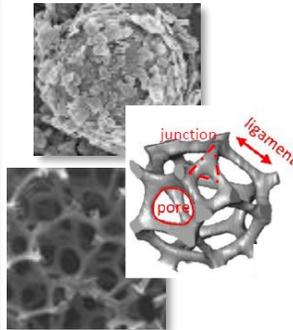
- Topologies
- Integration vs. Modularity

### Modeling



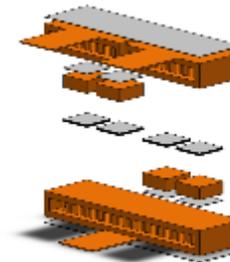
- Multi-Physics with Coupling
- ML-Based Optimization

### Materials



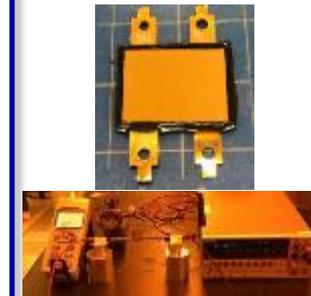
- EMC
- Die-Attach
- Substrates
- Wicks

### Integrated Cooling



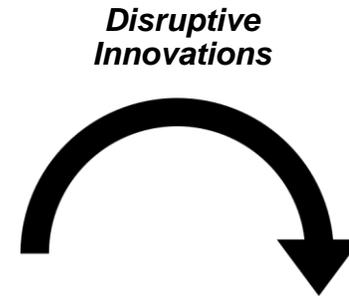
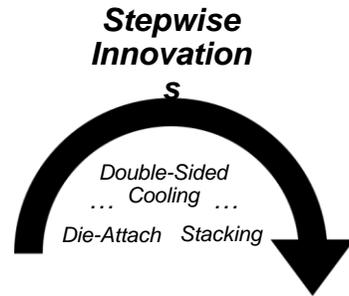
- In Current Terminals
- Multifunctional Structures

### Process & Reliability



- Leadframe-Based Pkg
- Scalability

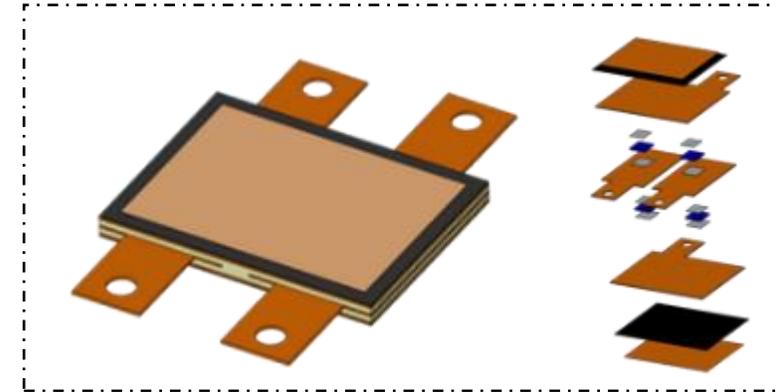
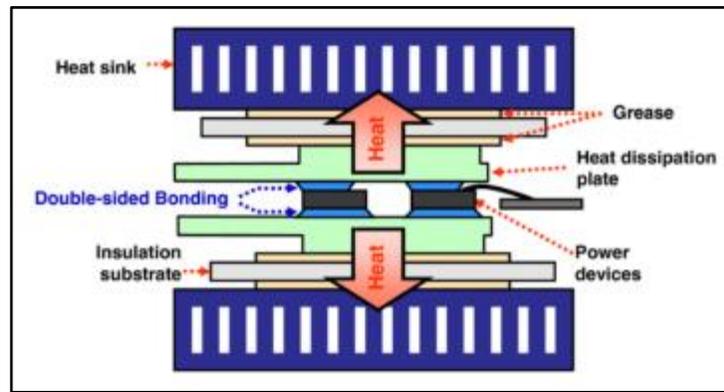
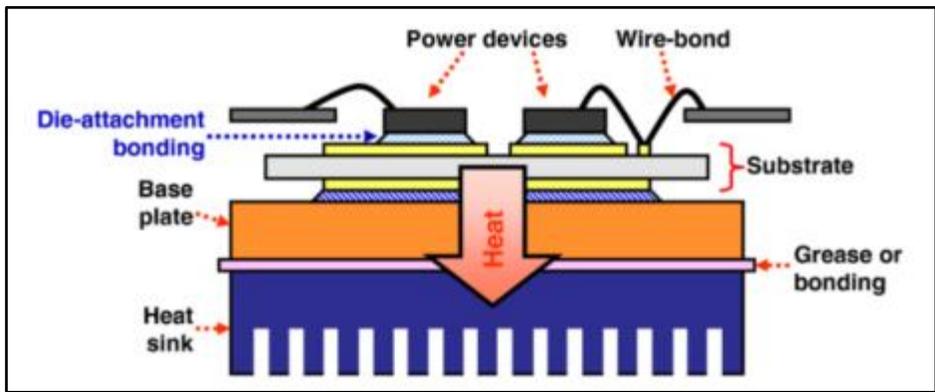
Through integration of active machine learning into the design and optimization process, it would be possible to hone on disruptive solutions to packaging technologies.



**Standard Packaging**

**Advanced Packaging**

?



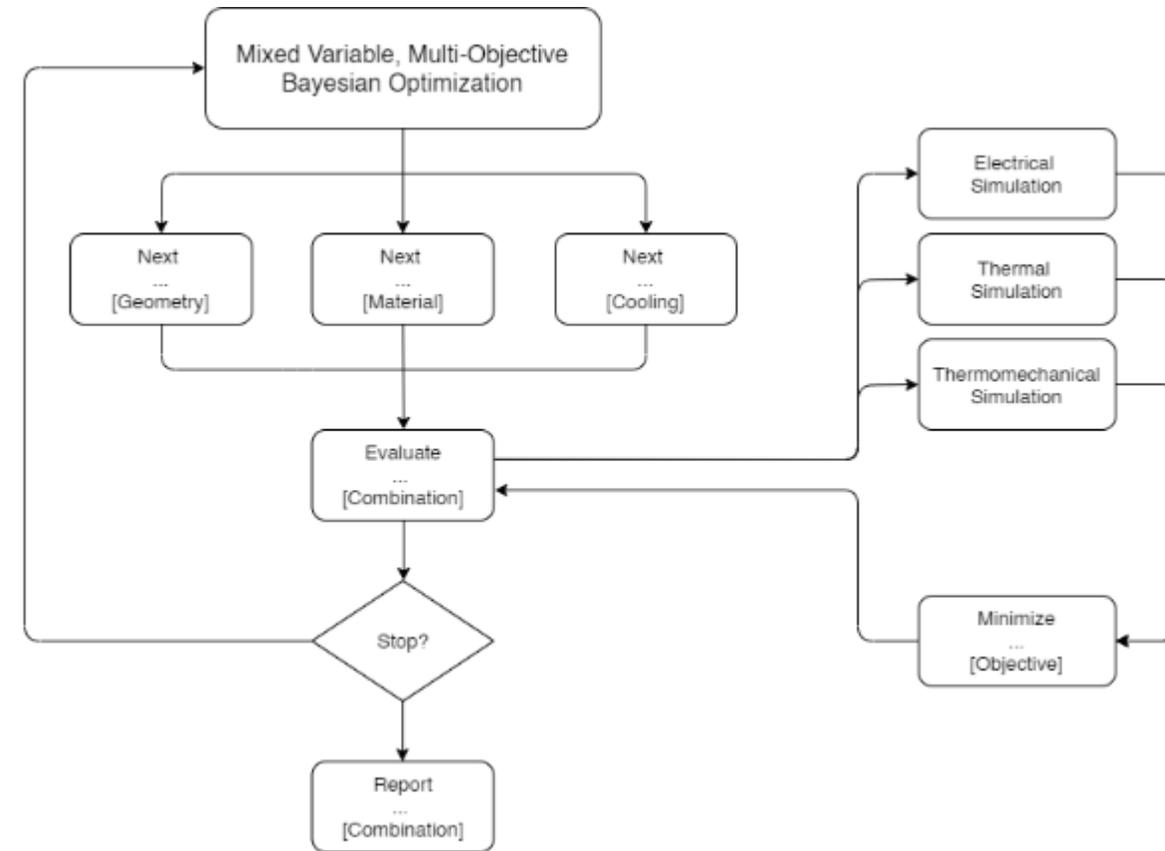
Package Parasitics (↓) Thermal Performance (↑) Reliability (↑) Manufacturability (↑) Integration (↑) Cost (↓)

In order to address the challenges of such a complex problem – multi-physics and multi-objective in nature – a novel tool has been developed to automate this exploration of packaging, through **Bayesian Optimization (BO)** based on **Gaussian Process (GP)**.

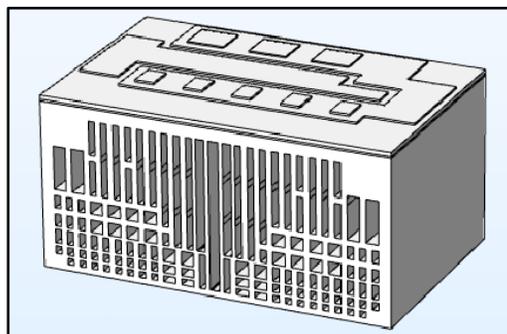
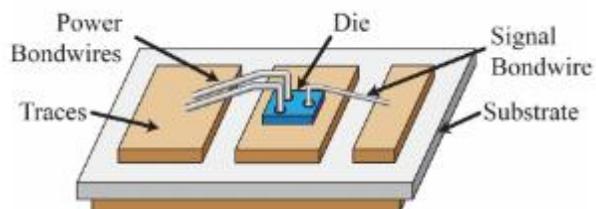
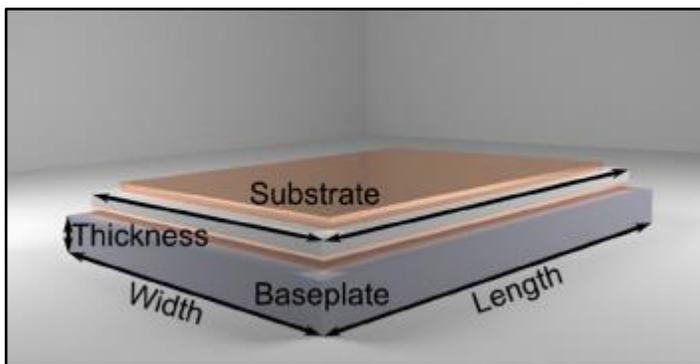
- **Bayesian Optimization (BO)** is a class of active machine learning algorithms that aims to minimize the number of evaluations required to find the global optimum of a computationally intensive function.
- **Gaussian Process (GP)** is a non-parametric model that can be used to place distributions over functions, providing a well-calibrated posterior in a scarce data regime.

In comparison to other tools, it offers many advantages.

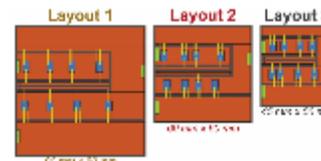
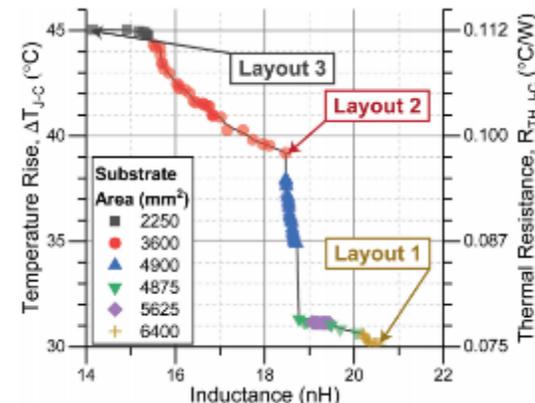
- **Reduced number of simulations**
- **Usage of high-fidelity finite element models**
- **Mixed variables, continuous or categorical types**
- **Multiple objectives**
- **Creation of accurate predictive model**



### Power Module Stack-Up



### Layout Optimization Pareto Frontier



	Optimization	Metric
Thermal	Die Area	Maximum Temperature
	Die Position	
	Trace Area	Temperature Rise
	Trace Position	
Electrical	Trace Width	Inductance
	Trace Length	

T. M. Evans et al., "PowerSynth: A Power Module Layout Generation Tool," *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5063-5078, 2019.

T. Wu, B. Ozpineci, M. Chinthavali, W. Zhiqiang, S. Debnath, and S. Campbell, "Design and optimization of 3D printed air-cooled heat sinks based on genetic algorithms," in *2017 IEEE Transportation Electrification Conference and Expo (ITEC)*, 22-24 June 2017 2017, pp. 650-655

## Optimization Methods

Regression Methods	Artificial Neural Networks
	Quadratic Response Surface
	Multiquadric Response Surface
	Response Surface
	Taylor Series Approximation
	Subapproximation Method
	Least-Squares Fit Method
	Design of Experiments
Optimization Algorithms	Genetic Algorithms
	Gradient Search Technique
	Conjugate Gradient Method
	Broyden-Fletcher-Goldfarb-Shanno Algorithm
	Pattern Search Method
	Simulated Annealing
	Subproblem Approximation and First-Order Methods
	Finite-Difference Gradient Method and Artificial Neural Network

## Limitation of Parameters

Methodology	Input	Output
Genetic Algorithms	6	2
Simulated Annealing	3	2
Genetic Algorithm + Simulated Annealing	3	2
Genetic Algorithm + Artificial Neural Networks	4	3
Design of Experiments	3	1
Design of Experiments + Least-Squares Fit Method	4	2
Force-Directed Algorithm	3	3
Force-Directed Algorithm + Fuzzy Logic	4	2
Cluster Growth Algorithm	3	3
Partition-Drive Algorithm	3	2

H. Hadim and T. Suwa, "Multidisciplinary Design and Optimization Methodologies in Electronics Packaging: State-of-the-Art Review," *Journal of Electronic Packaging*, vol. 130, no. 3, 2008.

I. Coulibaly, "METHODIC: a new CAD for electrothermal coupling simulation in power converters," in *IECON '98. Proceedings of the 24th Annual Conference of the IEEE Industrial Electronics Society (Cat. No.98CH36200)*, 31 Aug.-4 Sept. 1998 1998, vol. 4, pp. 2538-2542.

J. Z. Chen, Y. Wu, C. Gence, D. Boroyevich, and J. H. Bohn, "Integrated electrical and thermal analysis of integrated power electronics modules using ISIGHT," in *APEC 2001. Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.01CH37181)*, 4-8 March 2001 2001, vol. 2, pp. 1002-1006.

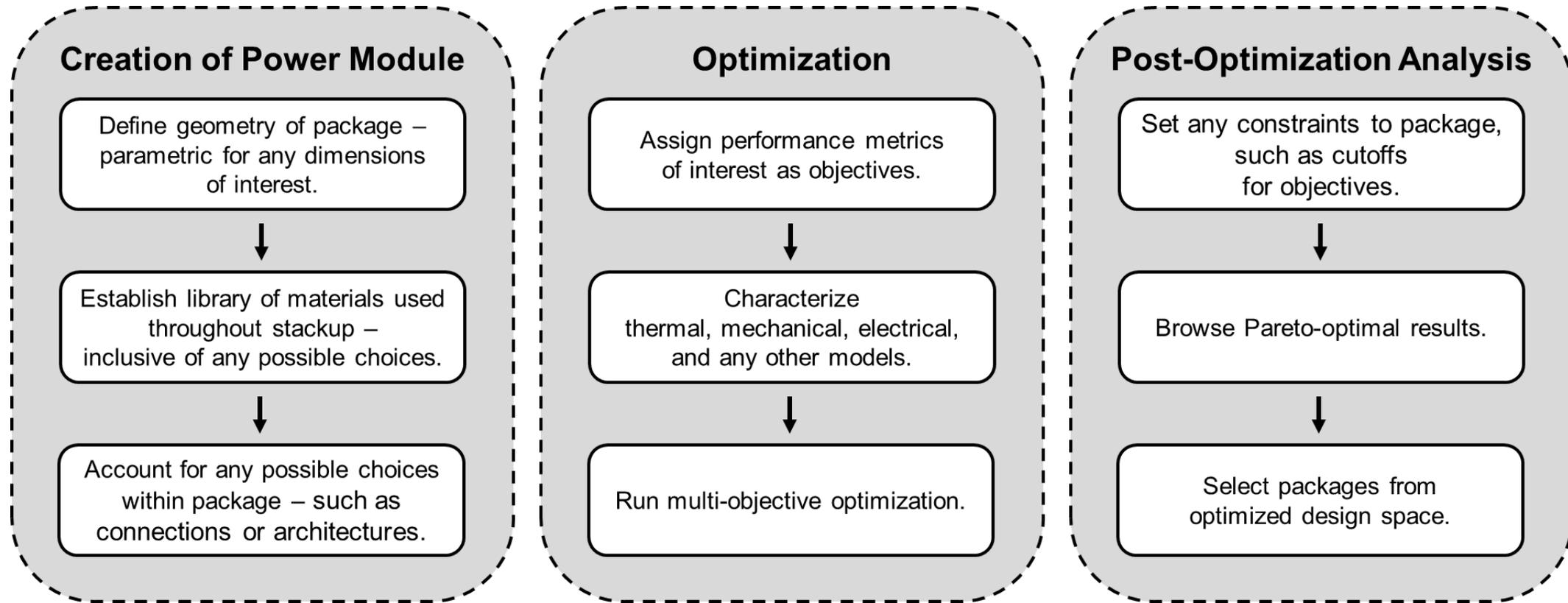
G. Xiong, M. Lu, C. Chen, B. P. Wang, and D. Kehl, "Numerical optimization of a power electronics cooling assembly," in *APEC 2001. Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.01CH37181)*, 4-8 March 2001 2001, vol. 2, pp. 1068-1073.

S. Sridhar and H. J. Eggink, "Dealing with uncertainty in power loss estimates in thermal design of power electronic circuits," in *Conference Record of the 1999 IEEE Industry Applications Conference. Thirty-Forth IAS Annual Meeting (Cat. No.99CH36370)*, 3-7 Oct. 1999 1999, vol. 2, pp. 1418-1422.

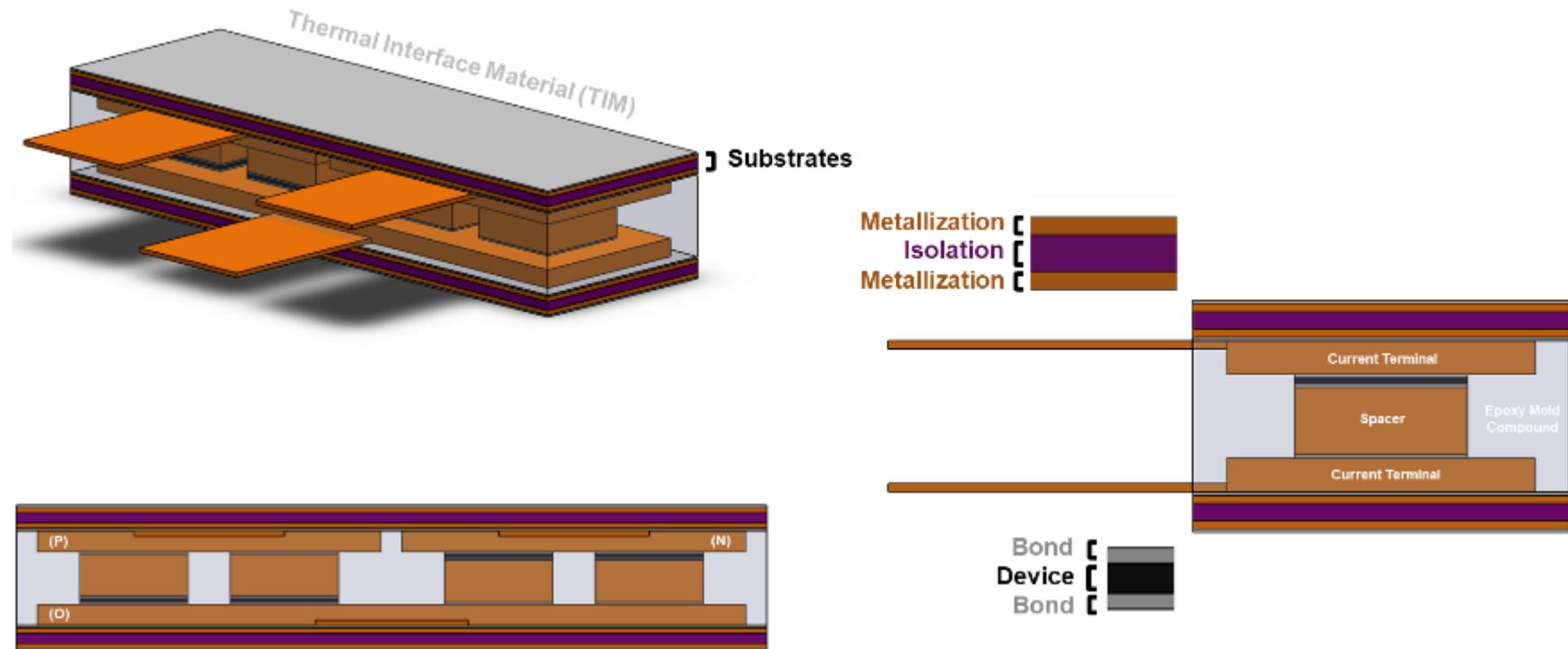
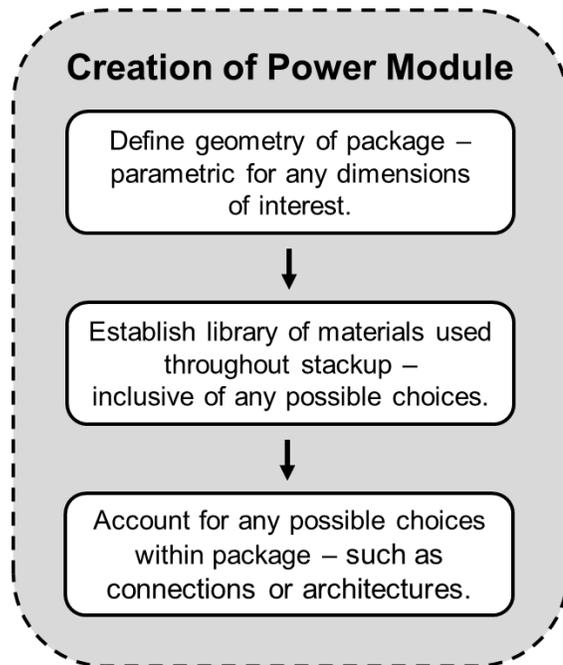
D. Gopinath, Y. Joshi, and S. Azarm, "An integrated methodology for multiobjective optimal component placement and heat sink sizing," *IEEE Transactions on Components and Packaging Technologies*, vol. 28, no. 4, pp. 869-876, 2005.

D. Gopinath, Y. K. Joshi, and S. Azarm, "Multi-objective placement optimization of power electronic devices on liquid cooled heat sinks," in *Seventeenth Annual IEEE Semiconductor Thermal Measurement and Management Symposium (Cat. No.01CH37189)*, 22-22 March 2001 2001, pp. 117-119.

<b>PowerSynth</b>	<b>Our Approach</b>
Few continuous parameters (4-5)	Many continuous parameters (8 and can go up to 40+)
Fixed package & materials	Include package & materials as categorical parameters (144 combinations and can go up to 1000+)
Core Algorithm: Genetic Algorithm (excessive simulations)	Core Algorithm: BO (reduced # of simulations, sensitivity analysis, manufacturing tolerances)
Works with approximate models.	Works with accurate FEM (Ansys)
Works only for certain package architectures (can't create approximate model for every package architecture).	Can include arbitrary packaging architectures as working directly with FEM.
Pareto Front (only full Pareto Front)	Pareto Front (full Pareto Front + ability to generate pairwise Pareto Front) + Constraints (Known and Unknown)



As a demonstration of this automated tool for design and optimization, a 50 kW SiC-based, half-bridge power card style module was used.



As illustrated in this schematic, the 3D geometry is fully parameterized in terms of layout, thicknesses, and materials.

## Creation of Power Module

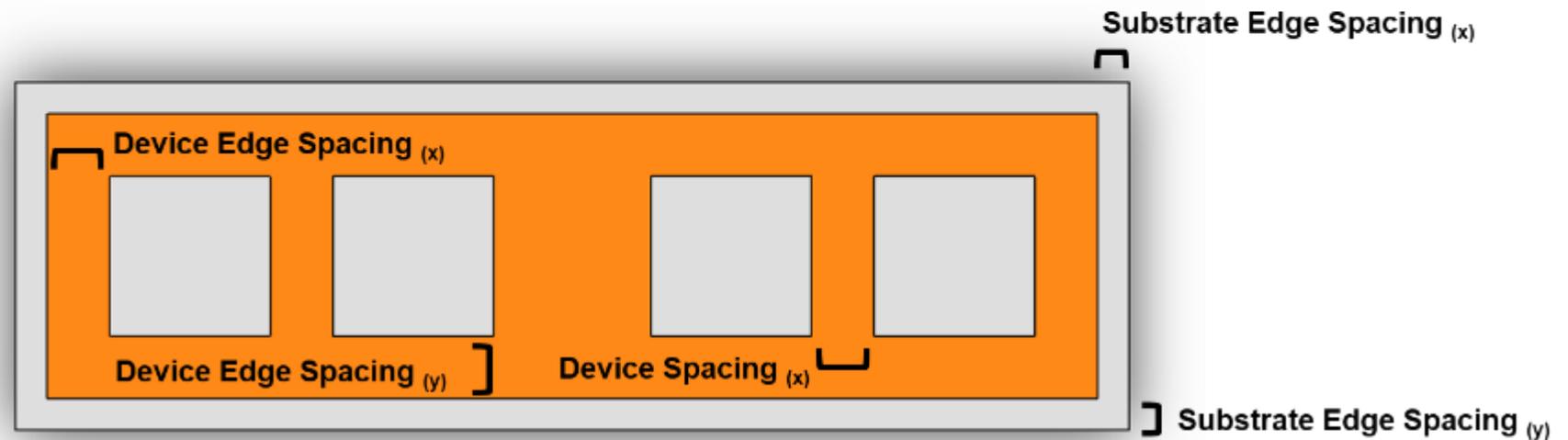
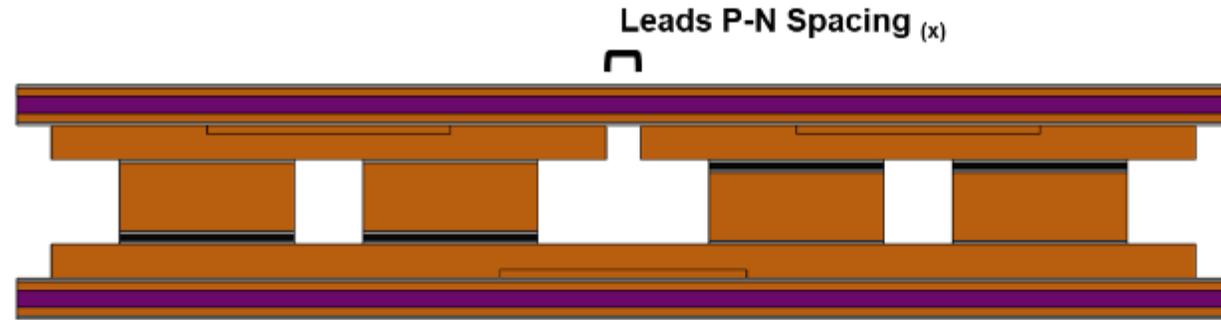
Define geometry of package –  
parametric for any dimensions  
of interest.



Establish library of materials used  
throughout stackup –  
inclusive of any possible choices.



Account for any possible choices  
within package – such as  
connections or architectures.



## Creation of Power Module

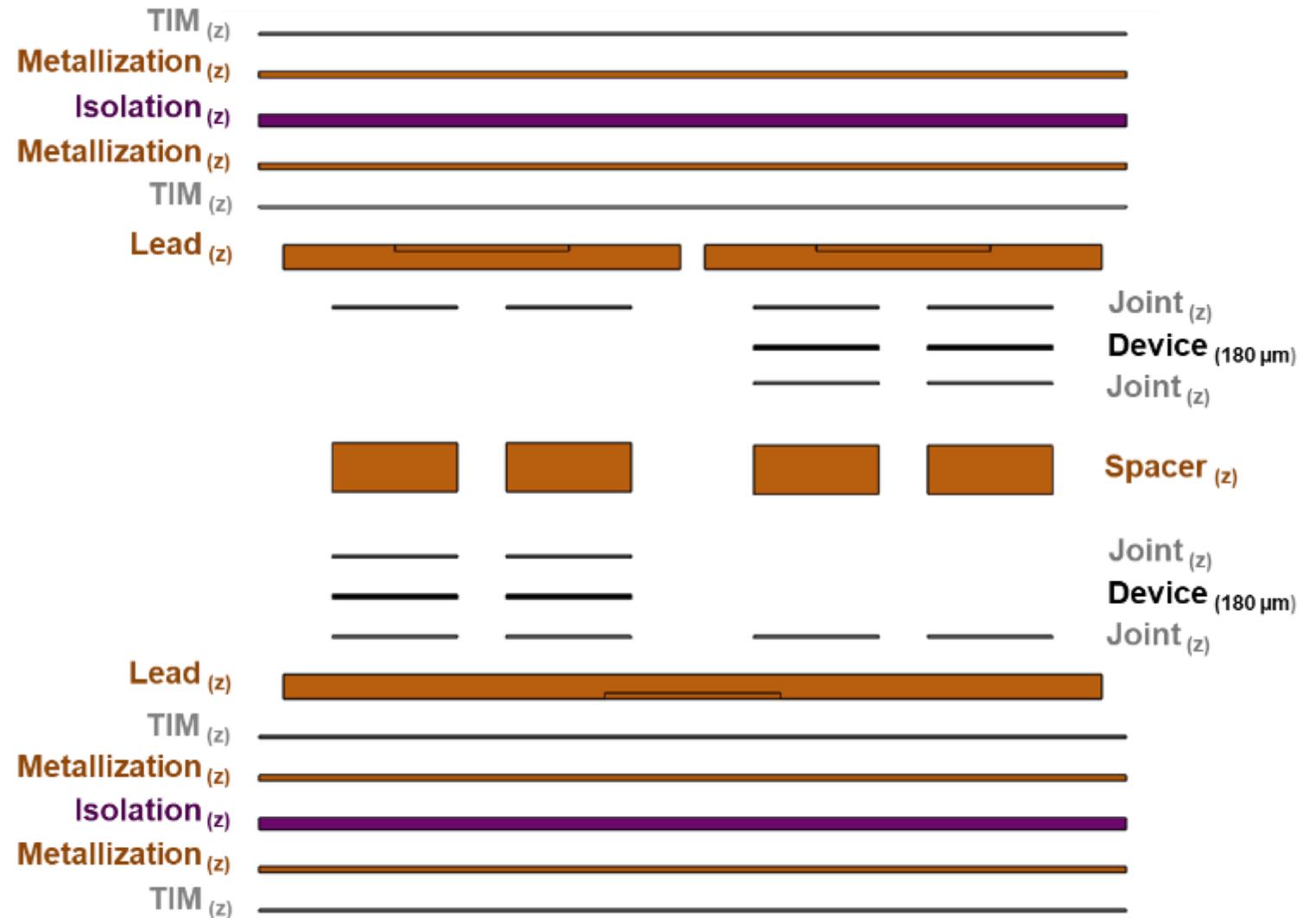
Define geometry of package – parametric for any dimensions of interest.



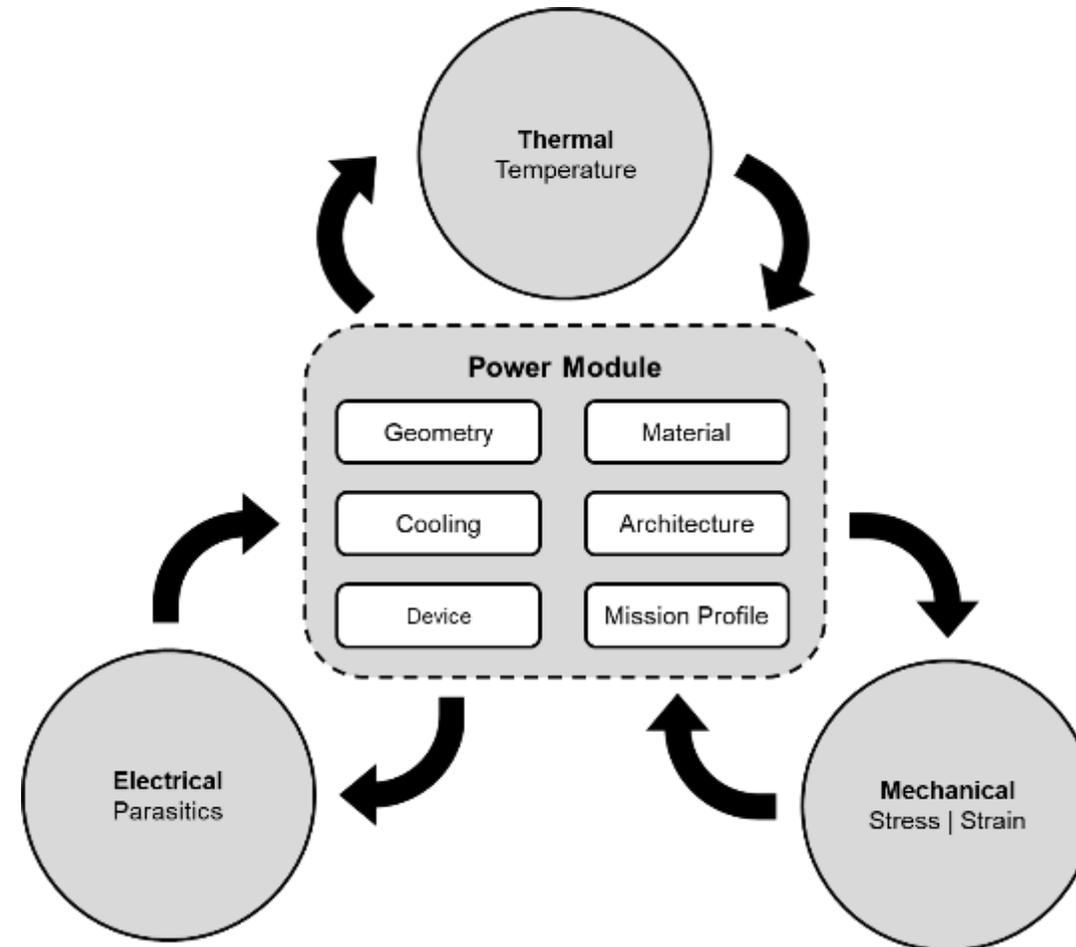
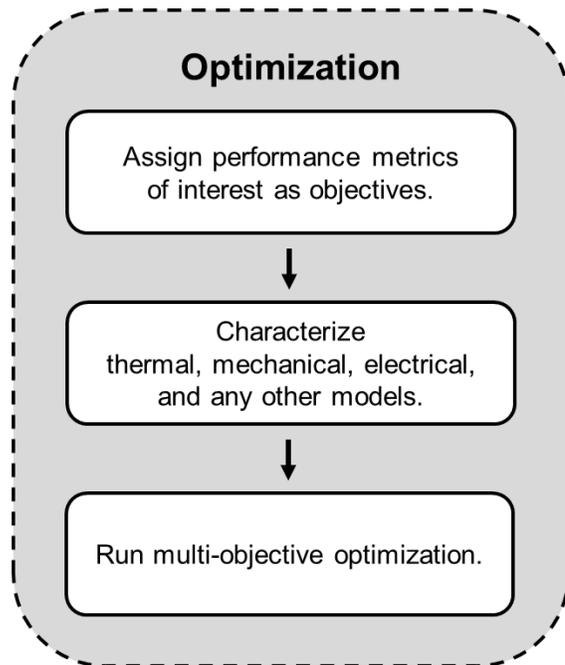
Establish library of materials used throughout stackup – inclusive of any possible choices.



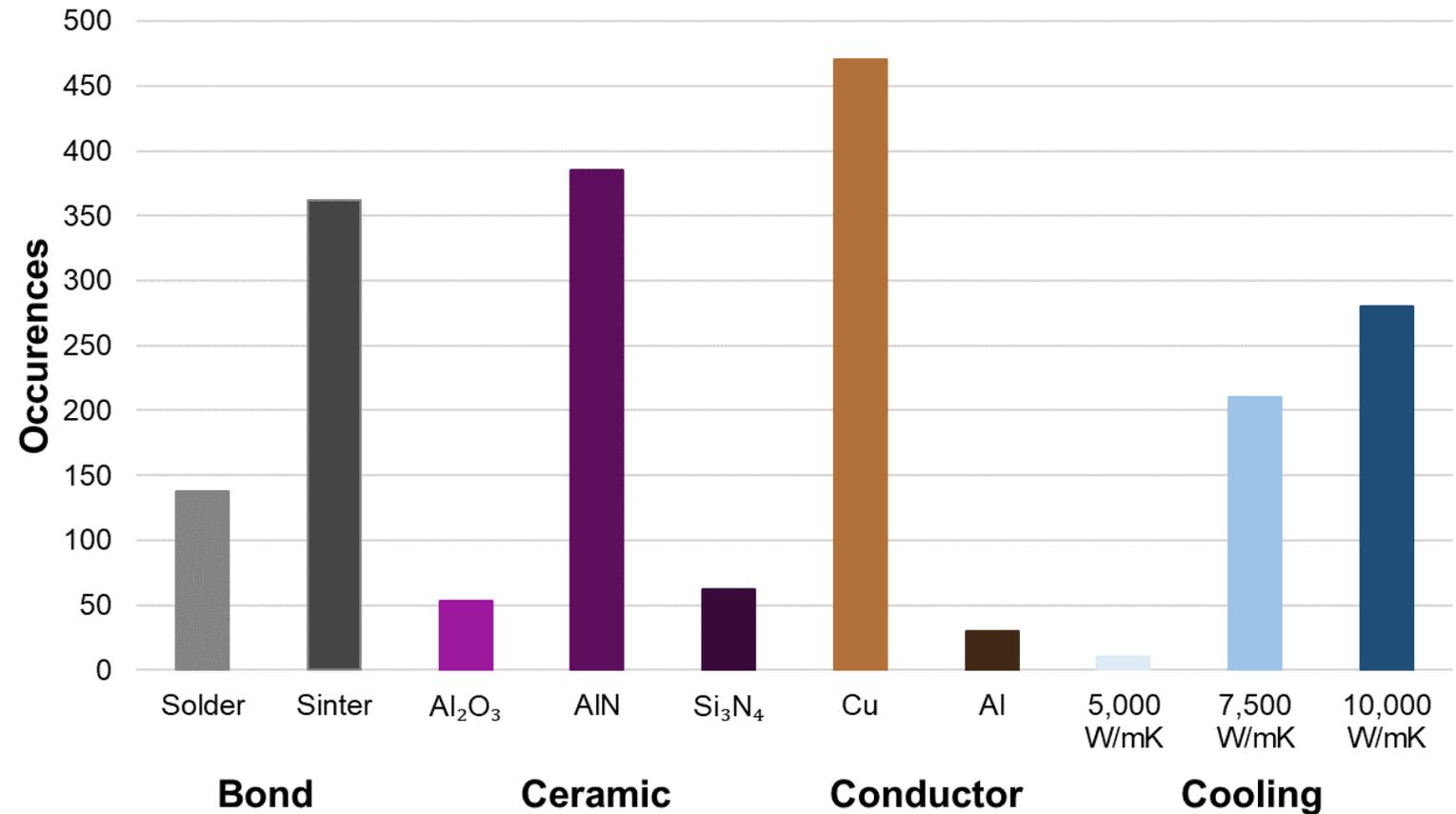
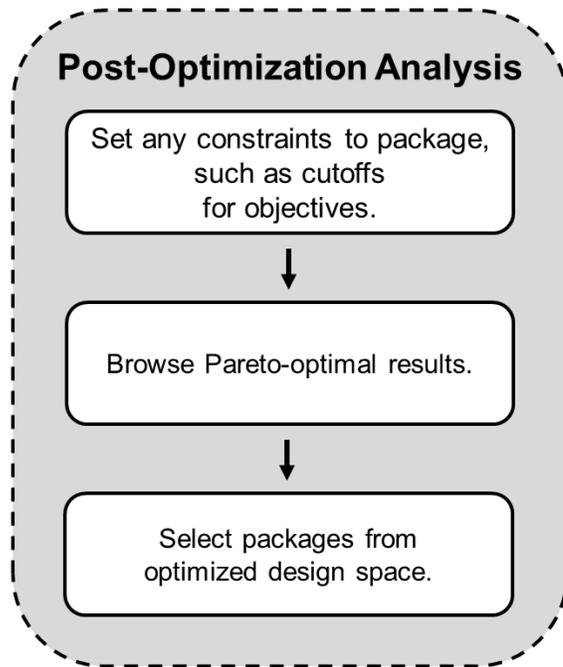
Account for any possible choices within package – such as connections or architectures.



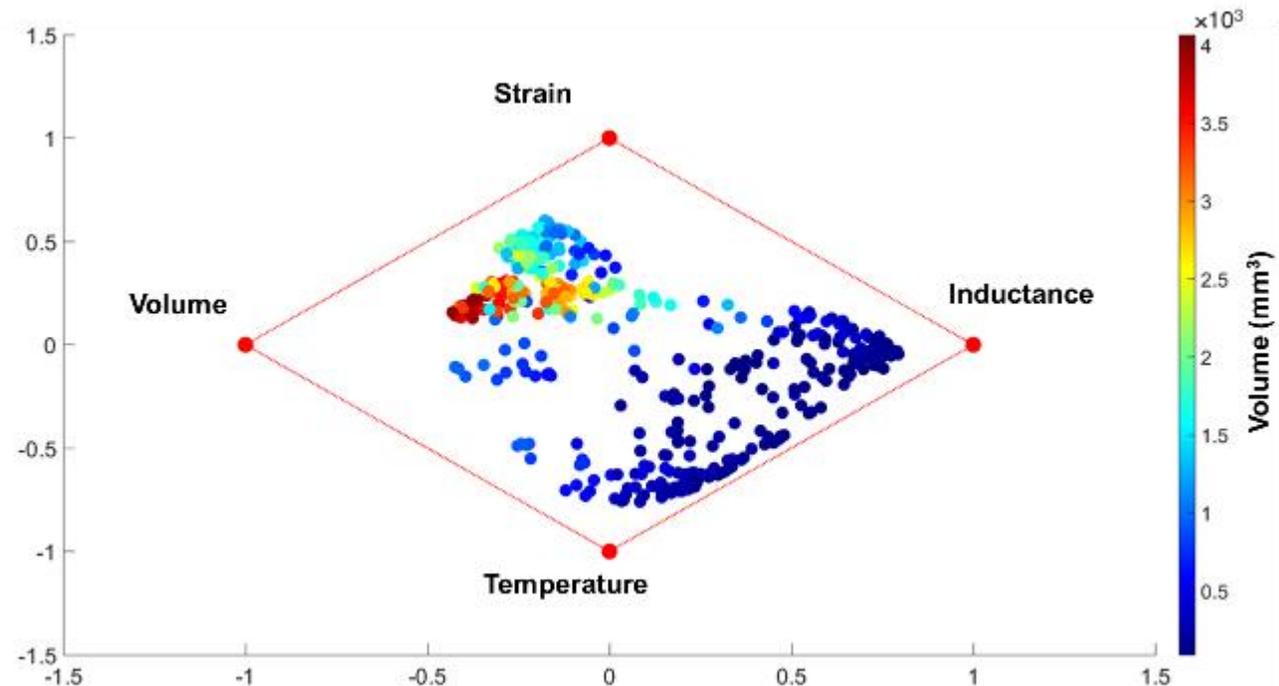
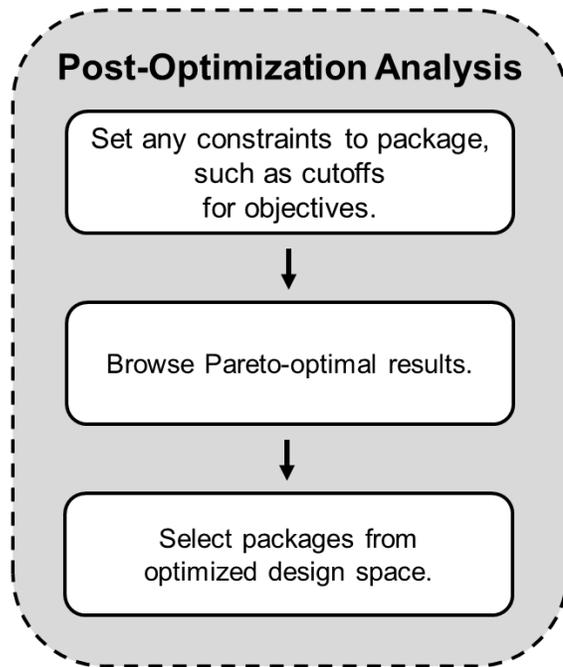
For this optimization, objectives for minimization include volume, junction temperature, strain in the joints, main power loop inductance.



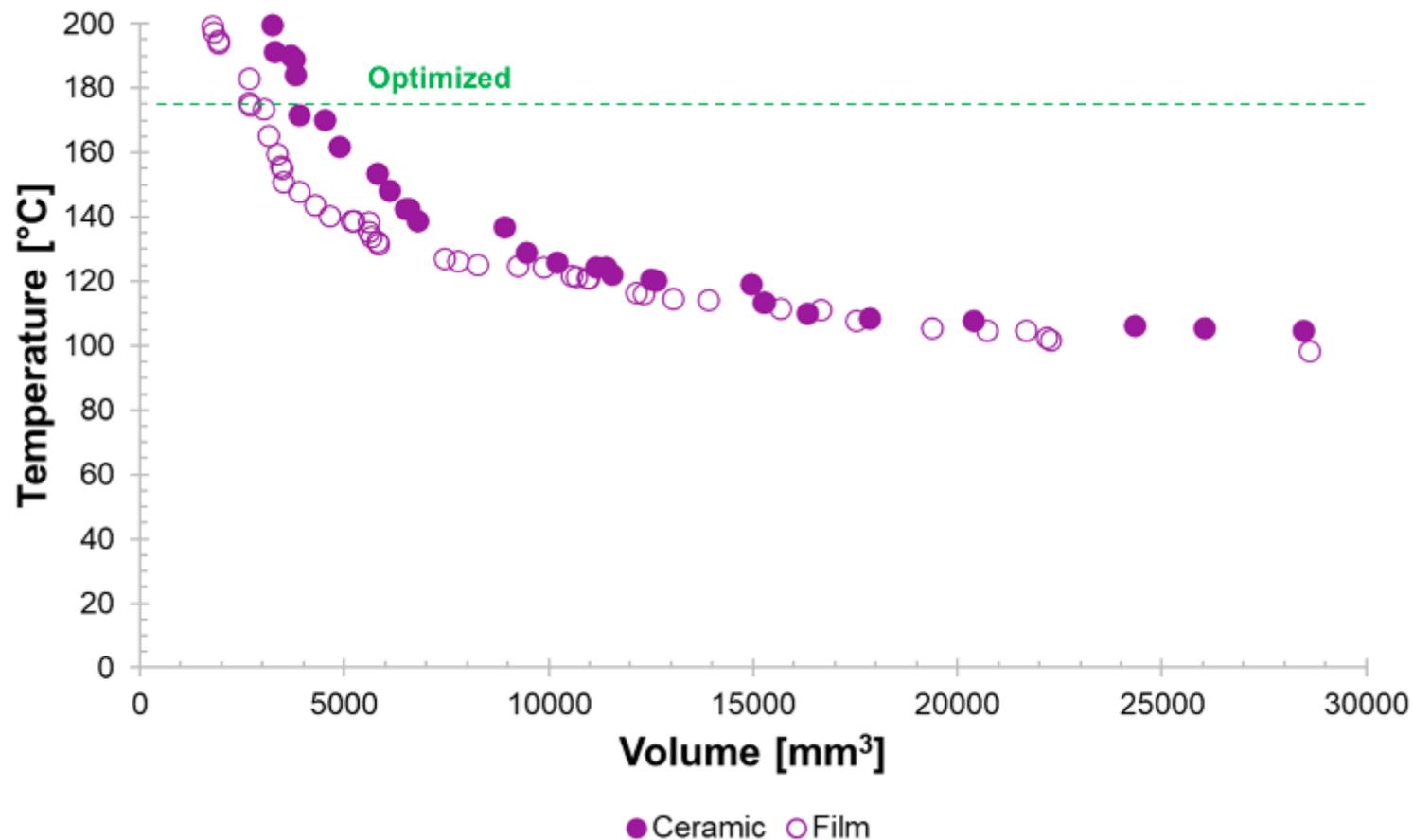
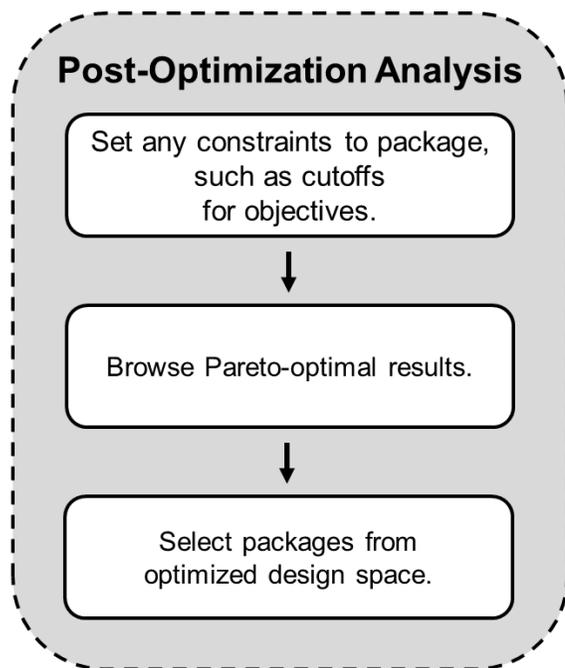
Based on the predictive model – built from simulations through machine learning – it is possible to sort through occurrences or choices that the algorithm have gravitated towards, among the optimized designs.

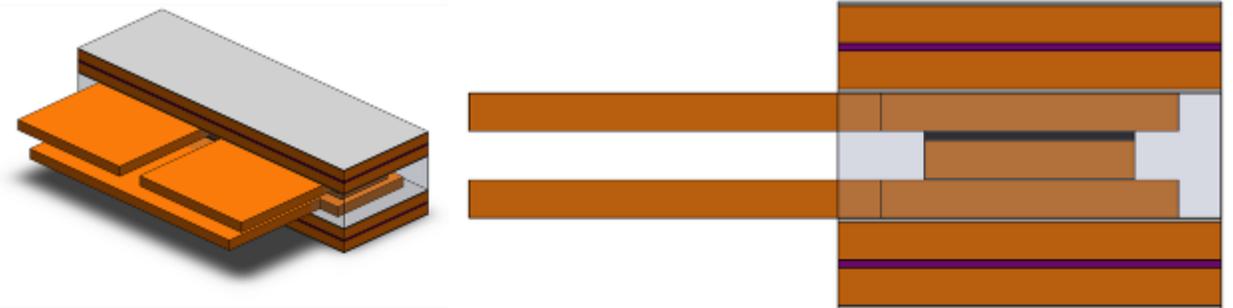
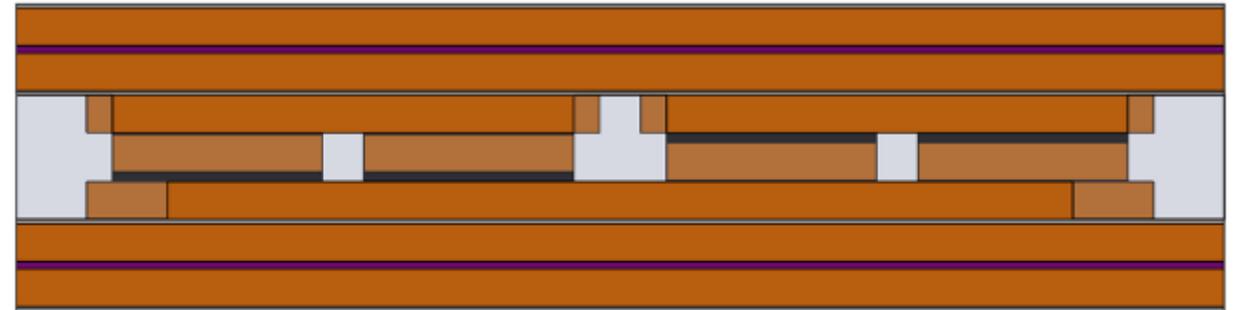
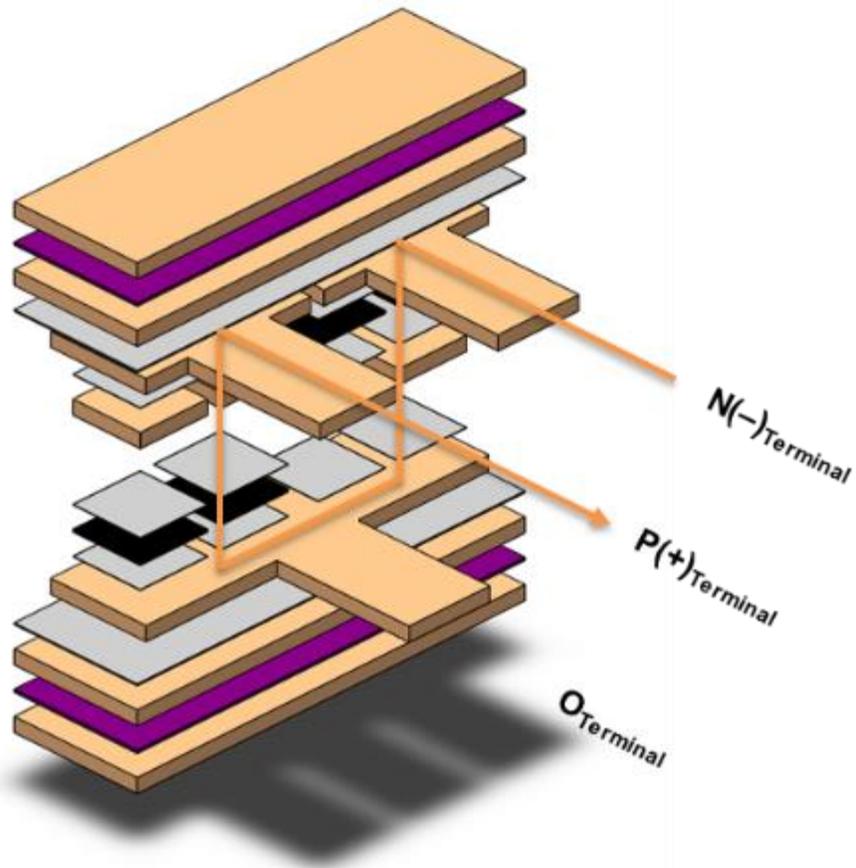


It is also possible to analyze the optimized designs in this radial visualization, relative to the objectives. Each anchor point is associated with a particular objective, and the positions of data points relative to that anchor point represents their performance relative to that particular objective.



For example, the closer a data point is to an anchor point – volume, temperature, strain, or inductance – the high its associated value is. Therefore, the most optimal designs would be in the center, in that it minimizes or balances for all the objectives.





### Objectives

Footprint – 29.4 mm × 9.3 mm  
Volume – 3586 mm<sup>3</sup> (-28%)  
Maximum Junction Temperature – 171°C  
Maximum Strain in Joints – 0.12% (-70%)  
Parasitic Inductance – 3.86 nH (-79%)

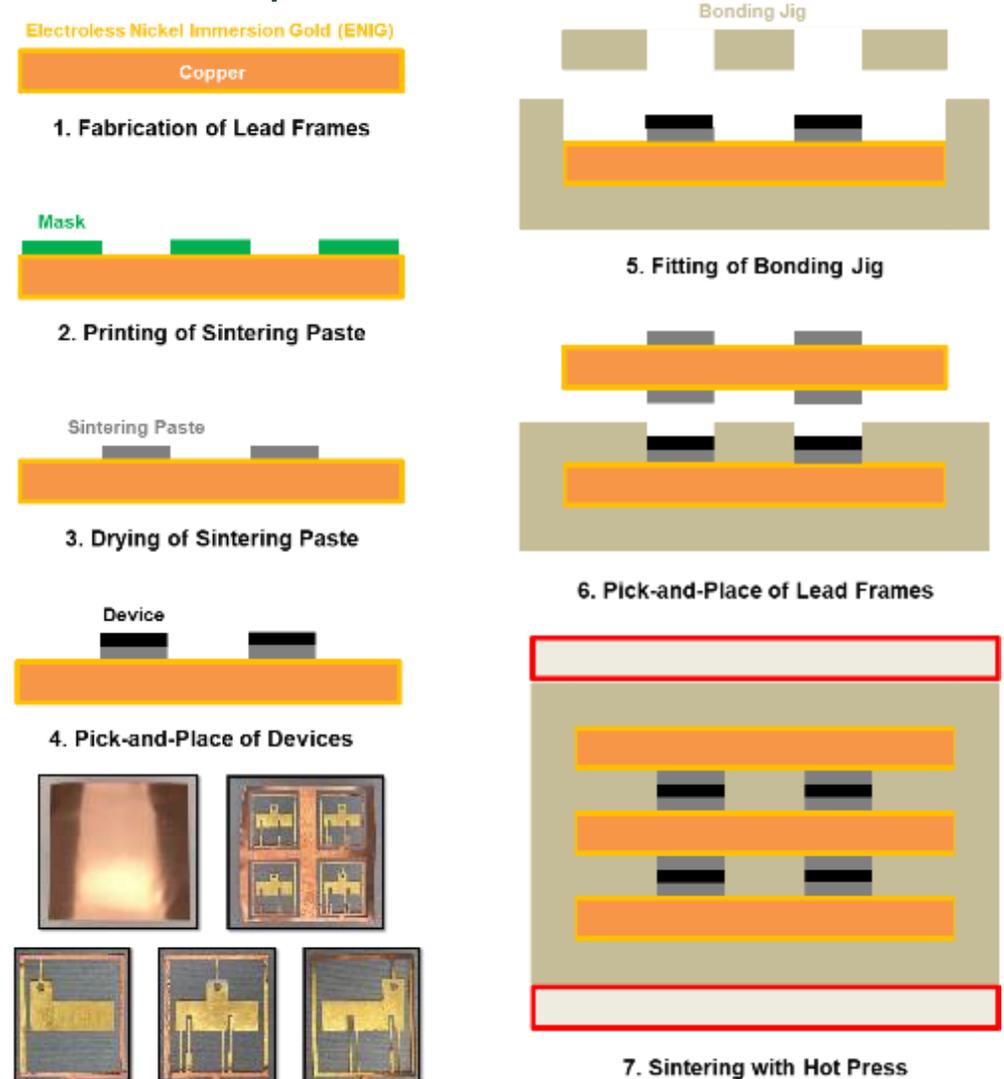
### Materials

Bond – Silver Sinter  
Conductor – Copper  
Isolation – Film  
Cooling – 7,500 W/m<sup>2</sup>K

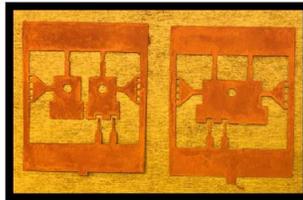
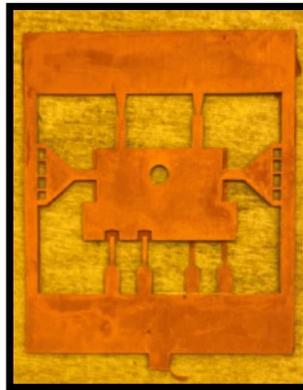
- 300mm cleanroom pilot facility and labs



- Fabrication process flow



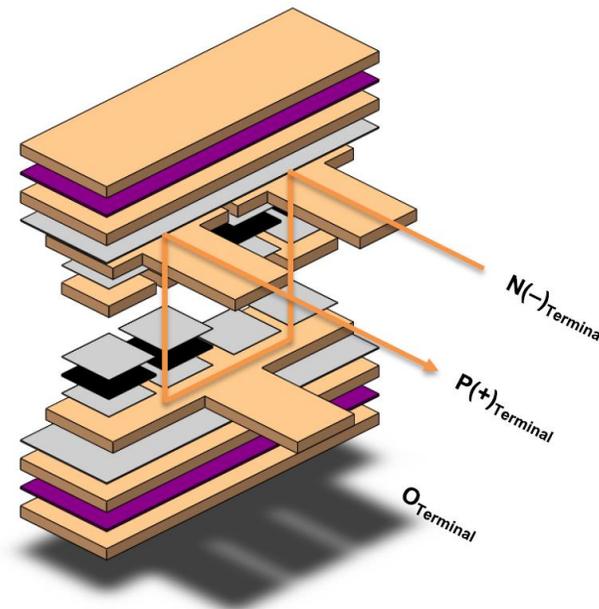
- For measurement of parasitic inductances, a package with a conductive test die was assembled



LCR Meter  
0.1% Accuracy, 30 ms/meas  
75 kHz – 30 MHz

Comparison of Test Dies  
@ 20 MHz

Pathway for Main Loop



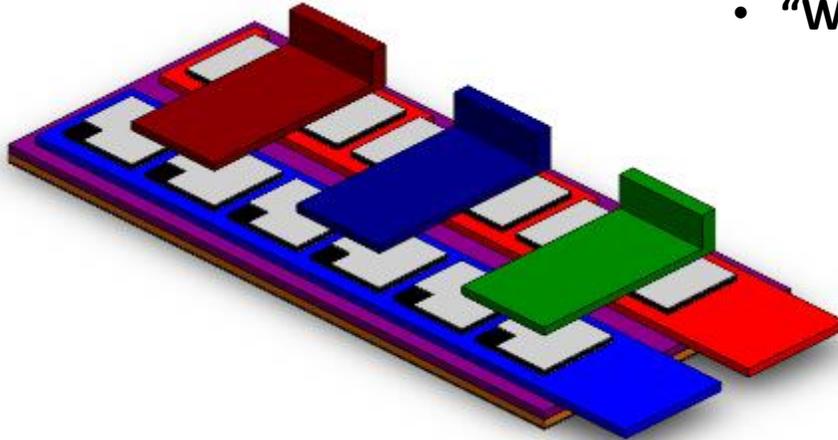
Results	Inductance
[Description]	[nH]
Simulation	3.86
Experimental	3.50

Percentage Difference  
(-9.8%)

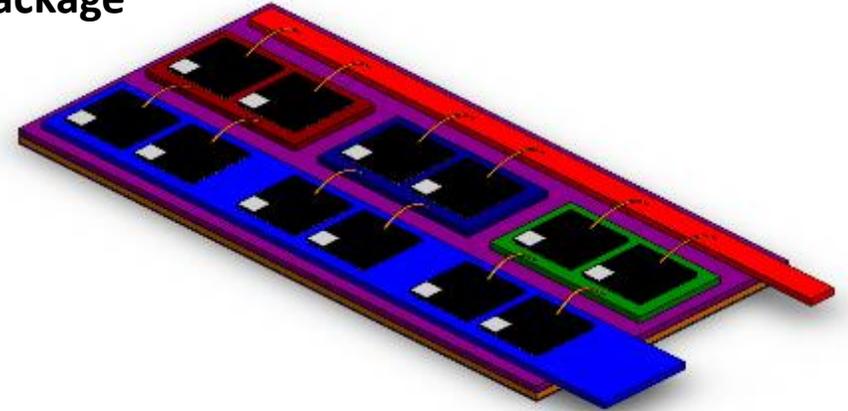
# Examples of Applications

Comparison of Arbitrary Package Architectures – Geometries for Full-Bridge Inverter Package

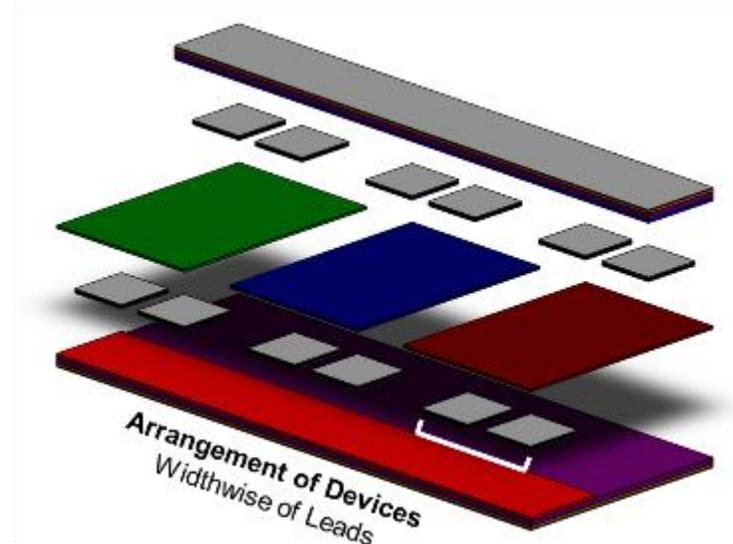
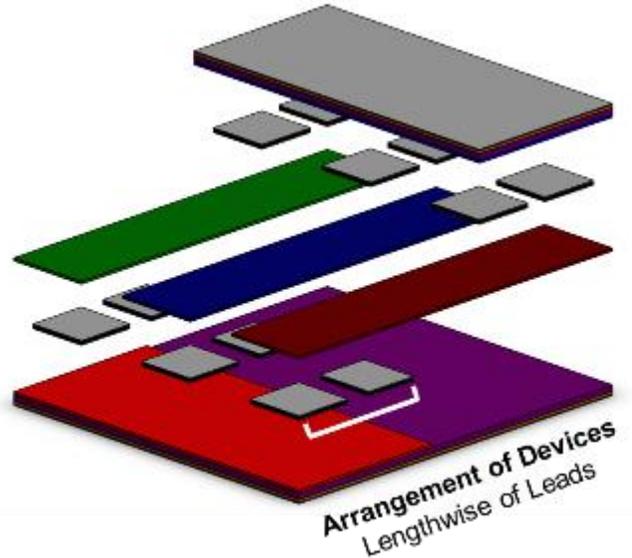
- “Planar” package



- “Wirebonded” package

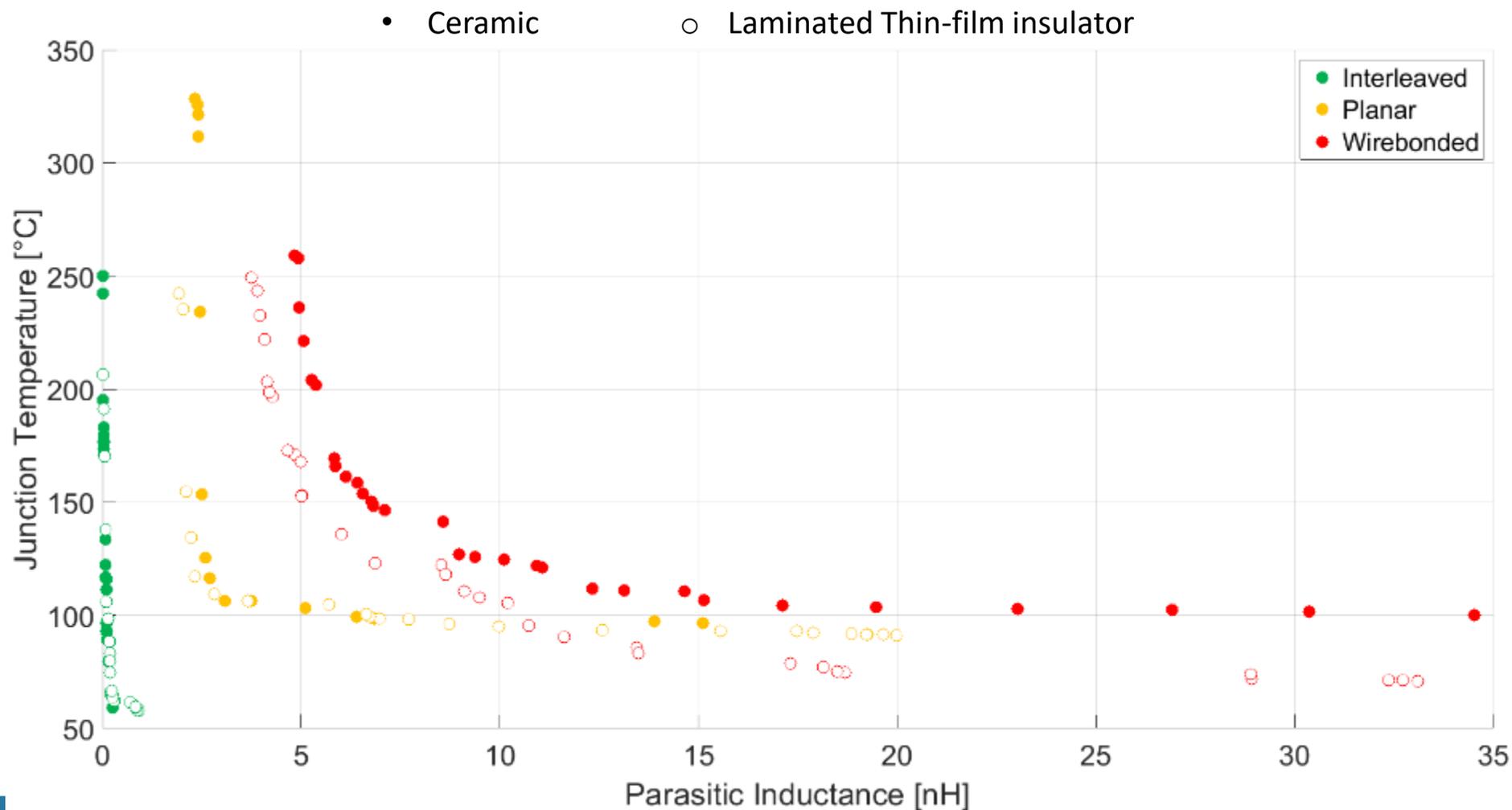


- “Interleaved” package with 2-level die stacking



# Examples of Applications

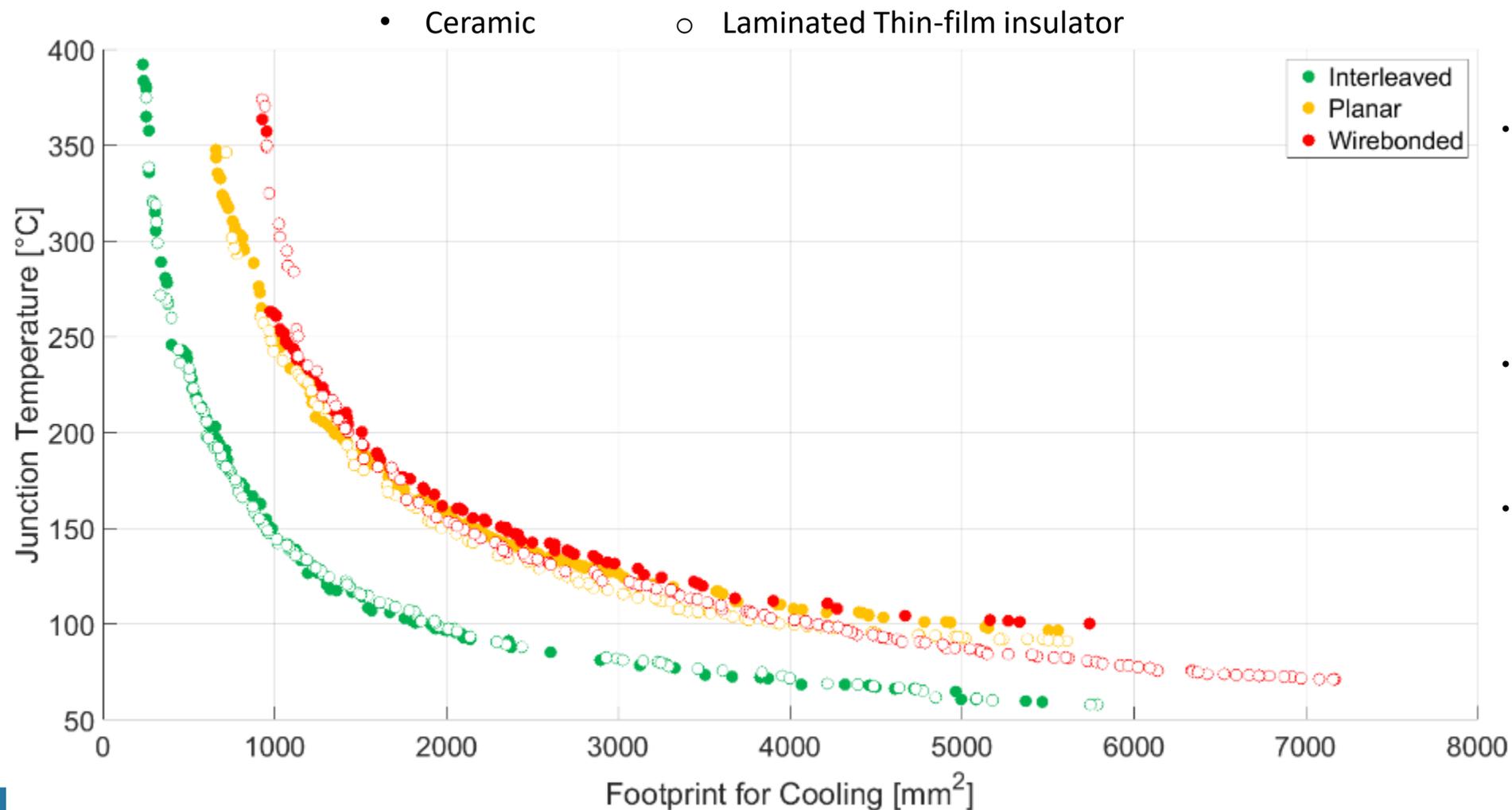
## Comparison of Arbitrary Package Architectures – Temperature & Inductance



- In comparison between the different approaches for isolation, it seems that packages with film-based isolation perform similarly if not superiorly in most cases.
- As illustrated in these Pareto fronts, packages with film-based isolation have more optimal solutions, in that their design are able to achieve lower maximum junction temperatures and parasitic inductances.
- Therefore, the use of film-based isolation can help to further the performance of packages, in surpassing important targets for these metrics.

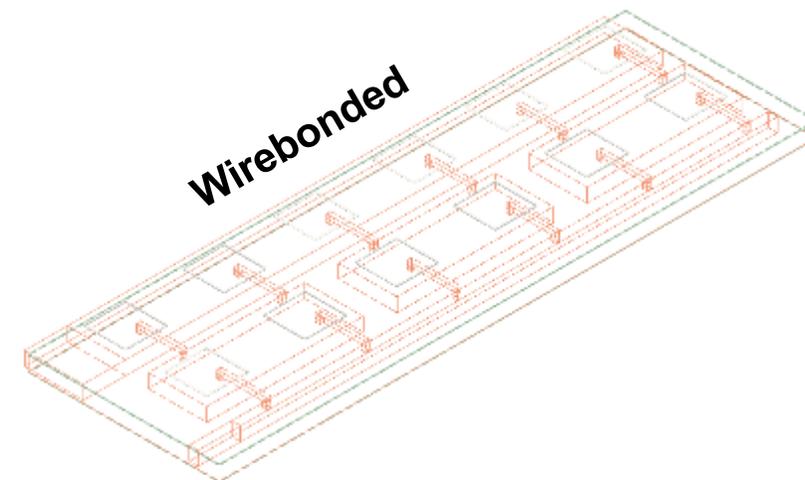
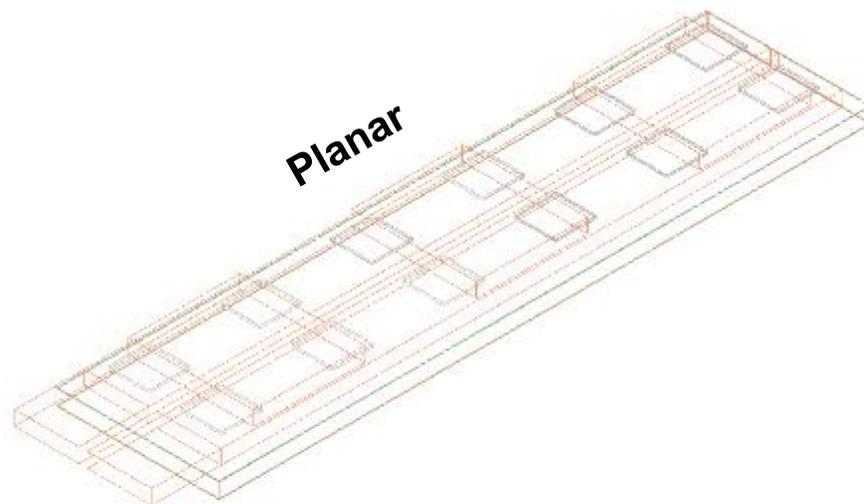
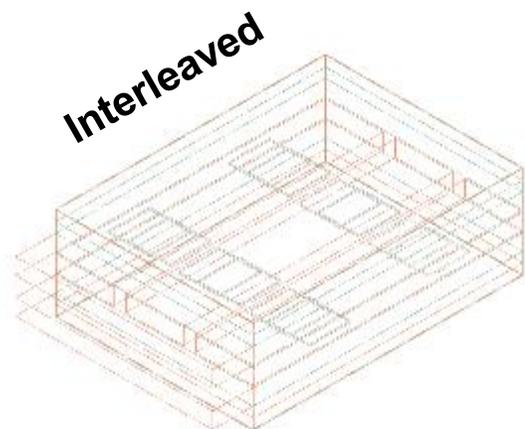
# Examples of Applications

## Comparison of Arbitrary Package Architectures – Temperature & Footprint



- In consideration of other metrics, such as maximum junction temperatures with respect to footprint for cooling, it is also demonstrated that film-based isolation perform similarly or superiorly.
- Advantages of film-based isolation include the elimination of costly or time-consuming processes for patterning ceramics.
- It is also shown that one of the major concerns with film-based isolation, in that they might detrimentally affect thermal performance, has been addressed through optimization.

# Examples of Applications Comparison of Arbitrary Package Architectures – Optimized Designs



Parameters	Objectives	Interleaved	Planar	Wirebonded
Electrical	Parasitic Inductance of Main Power Loop [nH]	0.68	2.91	8.71
Spatial	Footprint for Cooling [mm <sup>2</sup> ]	773	1655	1733
Thermal	Maximum Junction Temperature [°C]	173	172	175
Mechanical	Maximum Strain in Joints [%]	0.1	0.4	0.1

- Machine learning is key to developing efficient, integrated multi-physics co-design frameworks capable of exploring the entirety of the parameter space
- An automated tool relying on Bayesian optimization based on Gaussian process has been developed allowing for the first time the mixed-variable, multi-objective, multi-physics optimization of arbitrary power module architectures.
- Validation problem considered 20 continuous variables, 5 categorical variables, and 4 contradicting objectives – volume, parasitic inductances in the main power loop, maximum junction temperatures, and maximum strain in the joints – beyond the scope, scale, and capability of existing tools.
- Even with high fidelity finite element models, it still proved to be computationally efficient with 400 iterations – to converge and produce accurate predictive models – as achieved in just under 27 hours.
- Framework needs to further evolve to account for heterogeneous and system integration trends

