Inverter/converter power density and flexibility improvements through modularity and novel thermal management architecture

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MAREL POWER SOLUTIONS

OUTLINE

INTRO: POWER STACK DEFINITIONS AND BENEFITS

MAREL CORE POWER PACKAGE, DIE DENSITY AND SPECIFICATION

MITIGATING CTE MISMATCH IN DIE ATTACH

ISOLATED VS NON-ISO PACKAGE, THERMAL AND ELECTRICAL BENEFITS

RTH THEORETICAL SINGLE PATH VS SIMULATION

MODULARITY AND FLEXIBILITY IN NUMBER OF PACKAGES AND PHASES

BASELINE THERMAL SIM RESULT, DC CURRENT AND DISSIPATION

TRANSITION TO AC, PEAK CURRENT AND OFF TIMES

3-PH POWER DELIVERY, DOE TARGETS VS MAREL IN OVERALL POWER DENSITY

POWER STACK OVERVIEW

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INVERTER

POWER STACK

+

Control board, Software, Housing, & Capacitors

MAREL's Power Stacks use a '**MODULAR**' approach, enabling immediate, custom, and tuned solutions

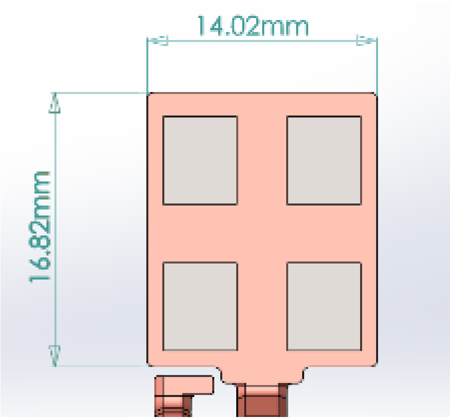
Miniaturized > 75% smaller > 50% lighter	**Integration** of drivers, sensors, etc
Security of Supply Use any die Use any technology	**Efficient** > 30% less thermal losses vs competition
Scalable 10kW to 1000kW+ 400V to 800V	**Fewer Power Semis** 25% to 50% fewer Or more power w/ same die

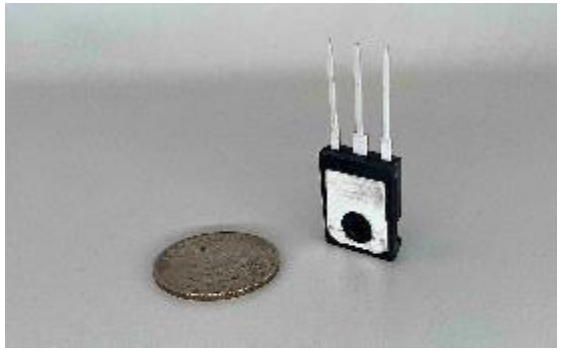
MAREL'S POWER SWITCH

Extremely Power-Dense and Sinter-able

1200V Silicon Carbide comparison, built with same die

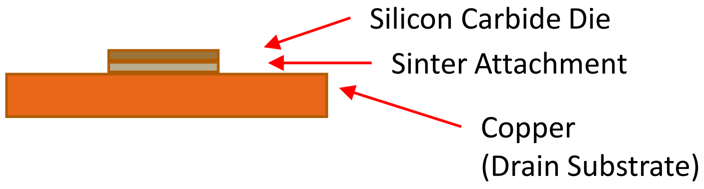
	Standard TO-247	Marel package
# of die	1	4
die attach method	solder drain wire bond source	sinter drain sinter source
cooling	single-side	double-side
Rds-on @ Tj=175C	28.8	7.2
Rth junction-case	0.27 C/W	<0.02 C/W
package dissipation @ Tj=175	208W	1280W
continuous drain current @ Tj=175C, Tcase=100C	85A	420A
package power path inductance	>15nH (typ)	<<1nH
sinterable package	no	yes
die flexibility	no	yes

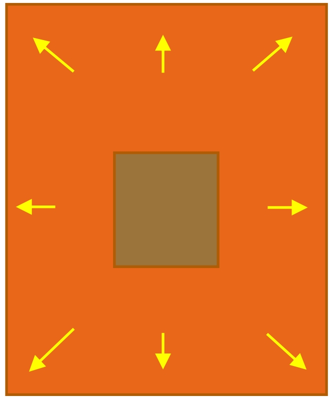




Density and performance of a custom power module in a flexible standard package

MITIGATING CTE MISMATCH





Copper expansion at a much faster rate will cause die delamination over time / temp cycling

Co-efficient of thermal expansion (CTE):
Silicon Carbide: 3.8 ppm/C
Silver Sinter: 20ppm/C
Copper: 16.5 ppm/C

Alloy or laminate combination with copper to create better thermal expansion match:
Tungsten: 4.5 ppm/C
Molybdenum: 5 ppm/C

	20K cycles	32K cycles	110K cycles
copper substrate	16% degrade	Fail	-
Marel substrate	0% degrade	0% degrade	0% degrade

ISO vs NON-ISO PACKAGES

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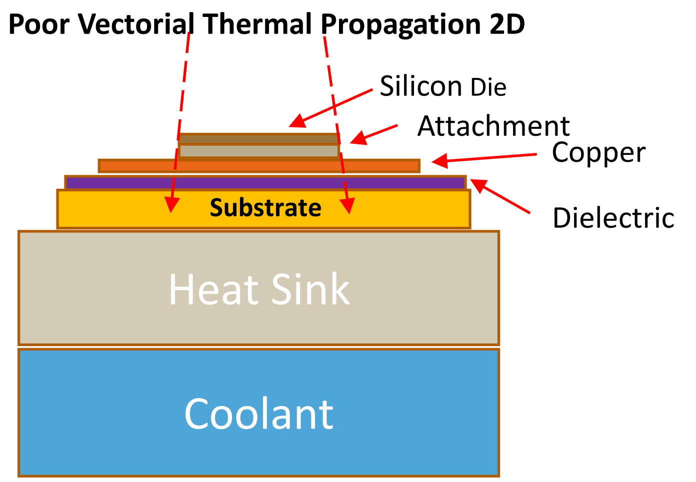
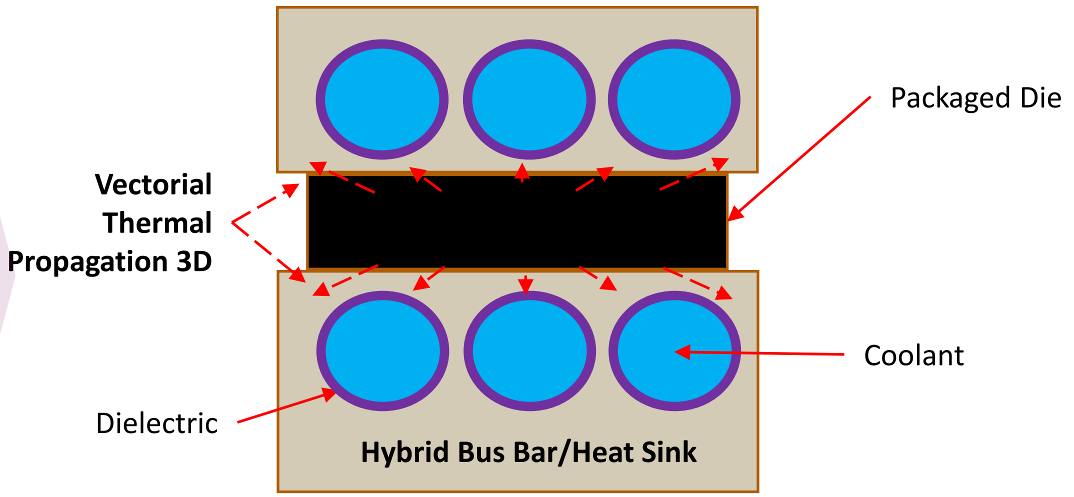




Typical isolated discrete package or module cooling:

Dielectric inside package, very close to die

Limited dielectric area

Thermal bottleneck close to heat source

Many attachment layers to degrade performance

Thermal capacitance effect is limited

Must create separate electrical paths (i.e. leads with parasitics)

Non-Isolated package with Marel cooling technology:

Dielectric as far from die as possible

Drastically increased dielectric area

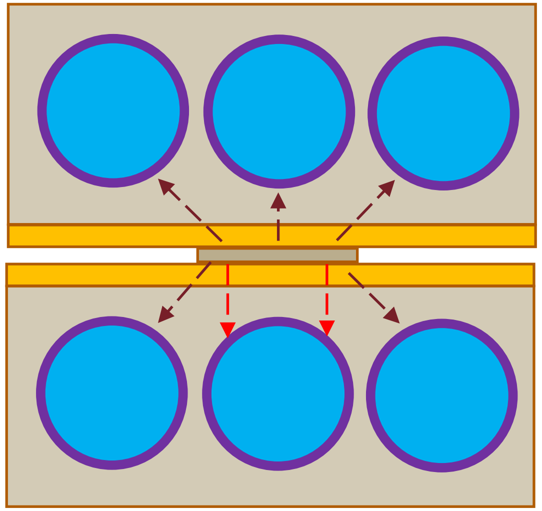
Thermal bottleneck mitigated

Very few attachment layers, all silver sintered

Thermal capacitance effect is maximized

Electrical and thermal paths are common, no separate leads to add inductance, resistance, etc.

THERMAL RESISTANCE (RTH) JUNCTION-COOLANT CONCEPT



Single die direct path calculation (conceptual):

Direct path calculation:

1 mm copper+ substrate @ 300 W/mK
.92+(.88 avg) = 1.8 mm copper @ 385 W/mK
.4 mm dielectric @ 170 W/mK (AlN example)

Rth = L / kA (L=thickness, k=conductivity, A=area)

.001 / (300*.00535*.00443) = .14 K/W
.0018 / (385*.00535*.00443) = .197 K/W
.0004 / (170*.00535*.00942) = .047 K/W
total = .384 K/W

However, this is only one of many paths!

Example single die simulation shows:
Rth = 38 K / 320 W = .119 K/W

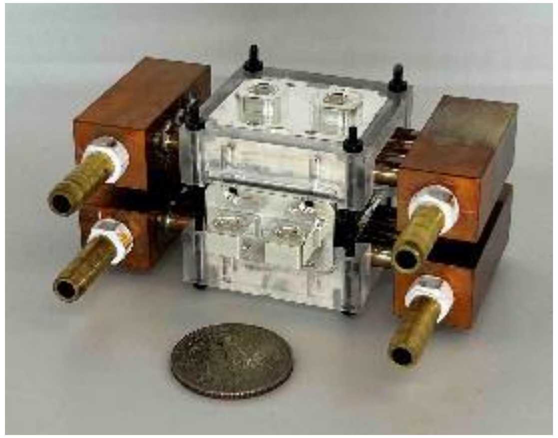
In a 4 die scenario, surface area will increase across the same material and thickness, as well as introduce even more complex thermal paths

Example 4 die simulation shows:
Rth j-coolant = 111 K / (4*320) W = .086 K/W

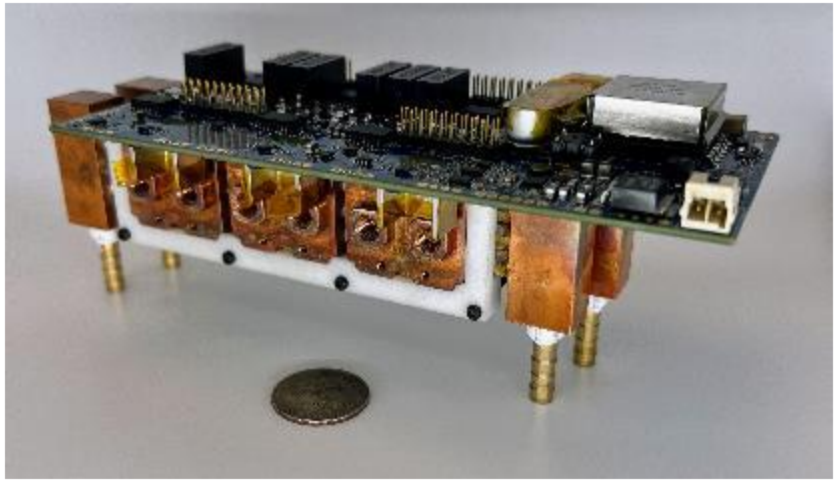
Example 8 die simulation shows:
Rth j-coolant = 111 K / (8*320) W = .043 K/W

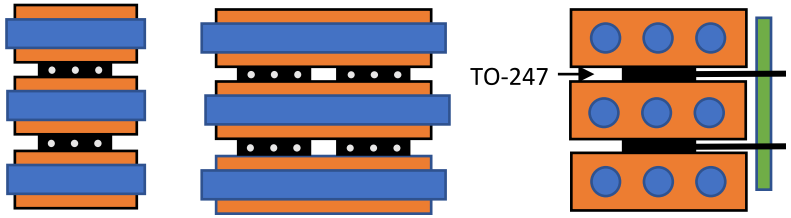
HALF-BRIDGE BUILDING BLOCK & COOLING CONCEPT

a 'MODULAR' approach, enabling immediate, custom, and tuned solutions

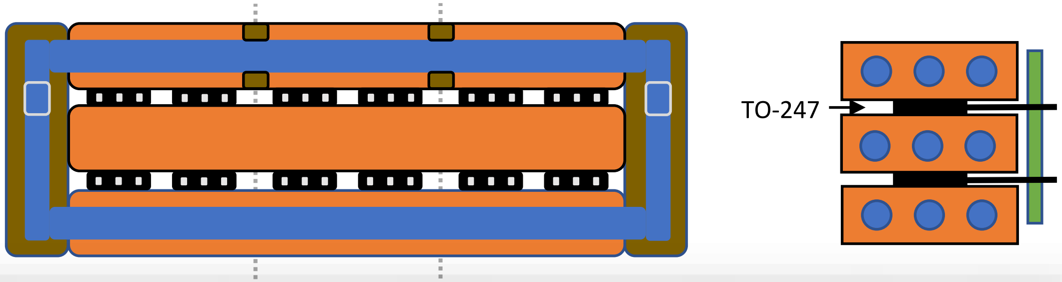


Any number of phases from the same building blocks





Double Sided Cooling

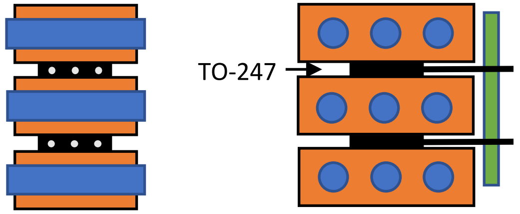


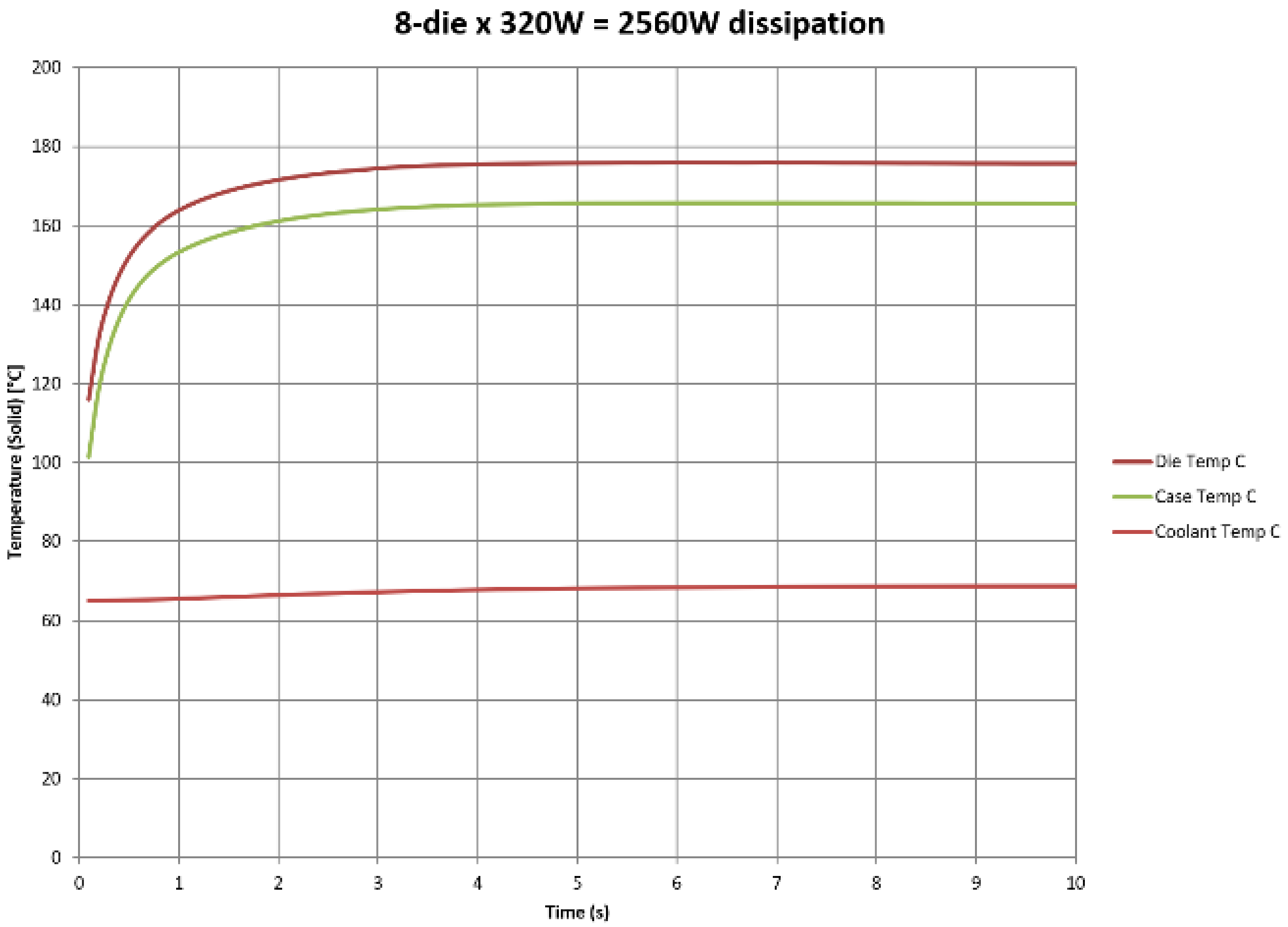
1-4 die per package, 1-16 die per switch configurable

STEADY STATE SIMULATION RESULT

8-die sim

- Inside half-bridge w/ manifold structure
- 10 L/min flow rate
- 8x SiC die, 320W dissipation each
- SiC die = 5.35mm x 4.43mm each
- Tj = 176C
- Tcase = 165C
- Tcoolant = 65C
- Rth junction-case = 0.009 C/W
- Rth junction-coolant = 0.043 C/W
- Amp/die = sqrt(320W/.0288Ohm) = 105A
- 420A @ 175C in Marel package

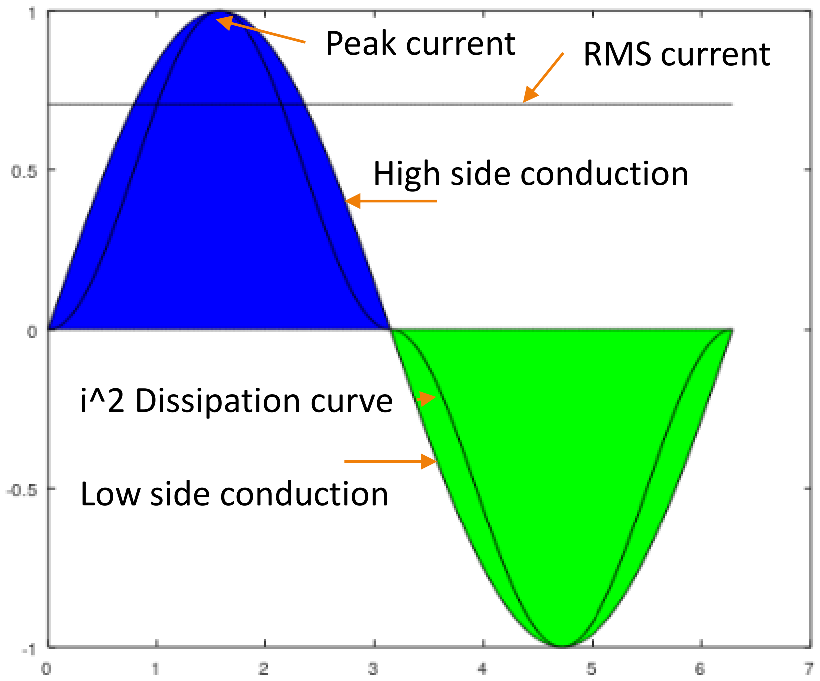


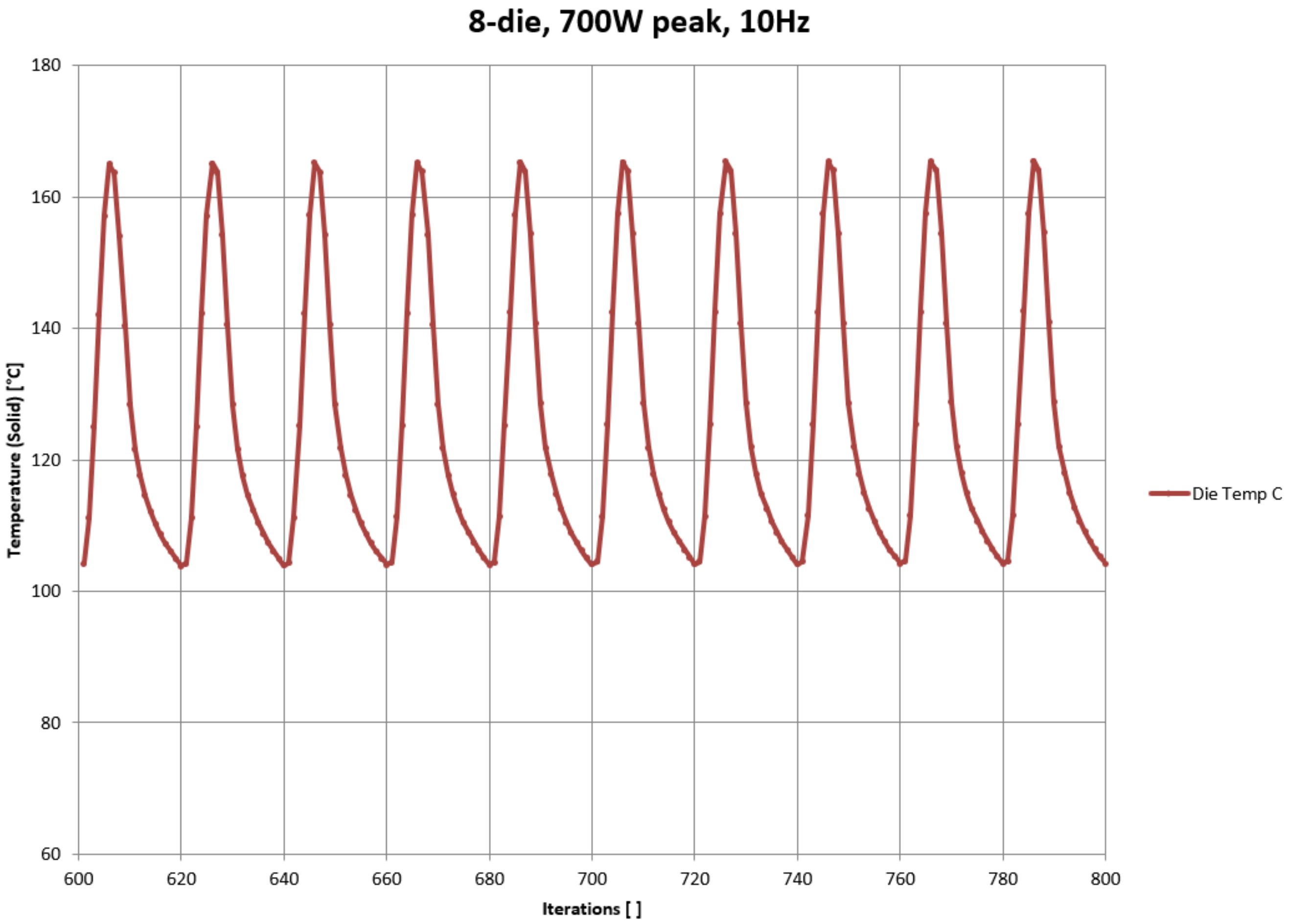


ALTERNATING CURRENT (AC) SIMULATION RESULT

8-die AC sim

- Switch modeled with sinusoidal^2 dissipation curve for half cycle, then off for half cycle (see picture)
- 8x SiC die, 700W peak dissipation each
- 10 Hz operation, low speed is worse case
- Tj = 165C, Tcoolant = 65C
- If we assume roughly 15% switching loss:
- Peak Amp/die = sqrt(595W/.0288Ohm) = 144A
- RMS Amp/die = 144A / sqrt(2) = 102A





POWER DENSITY TARGETS

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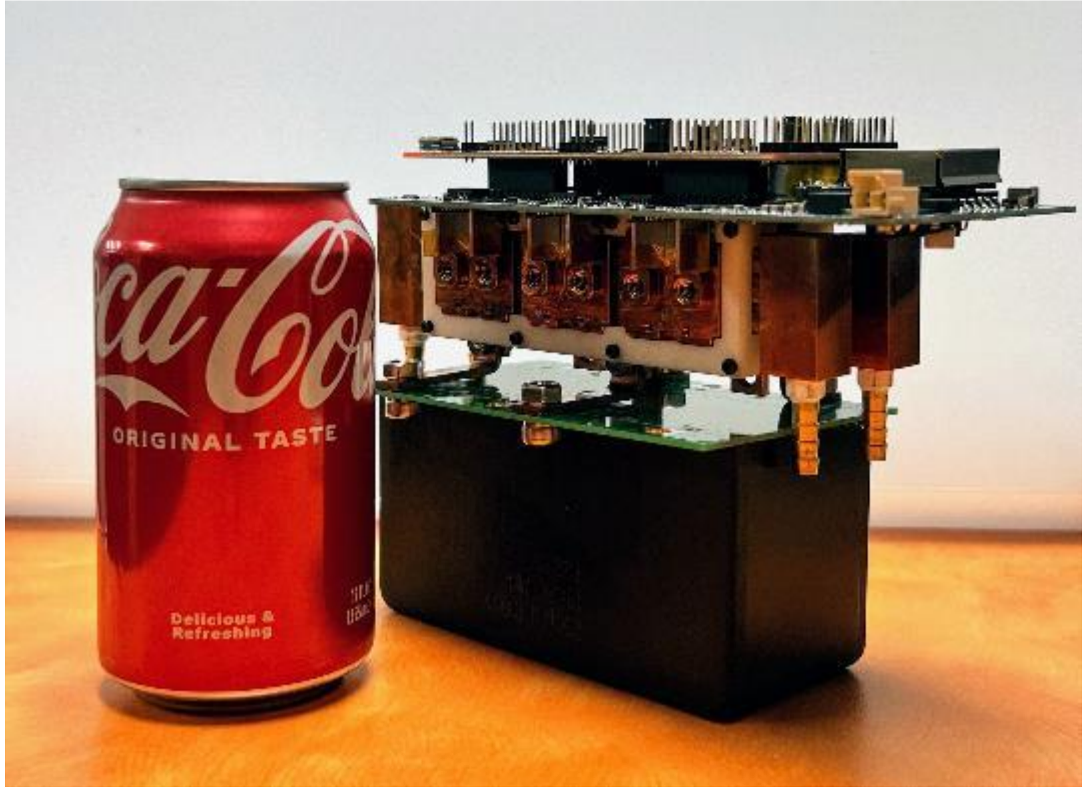
Power density in a 3-ph inverter

- Photo to the right is prototype Marel full 3-phase inverter, minus housing
- Estimated volume with housing is 2 Liter
- Using previous AC simulation as a baseline:
- RMS Amp per 8-die switch = 102A *8 = 816Arms
- With an 800V dc bus, 565.7Vrms
- 3 phase power = 816Arms * 565.7Vrms * sqrt(3) * 0.9 PF
    - ~= 720KW for a pure sinusoidal drive
- Power density ~= 720KW/2L = 360 KW/L



US Department of Energy targets for vehicle inverter

- Power Density: 100KW/L by 2025
- Cost: $2.7/KW by 2025

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