

Georgia Tech



MICROSYSTEMS  
PACKAGING  
RESEARCH  
CENTER

# Greetings !

## Future Packaging and Power Integration Emergence of Indian Electronics

Prof. Rao R. Tummala

Founding Director and Emeritus Professor

3D Electronic Systems Packaging Research Center(PRC)

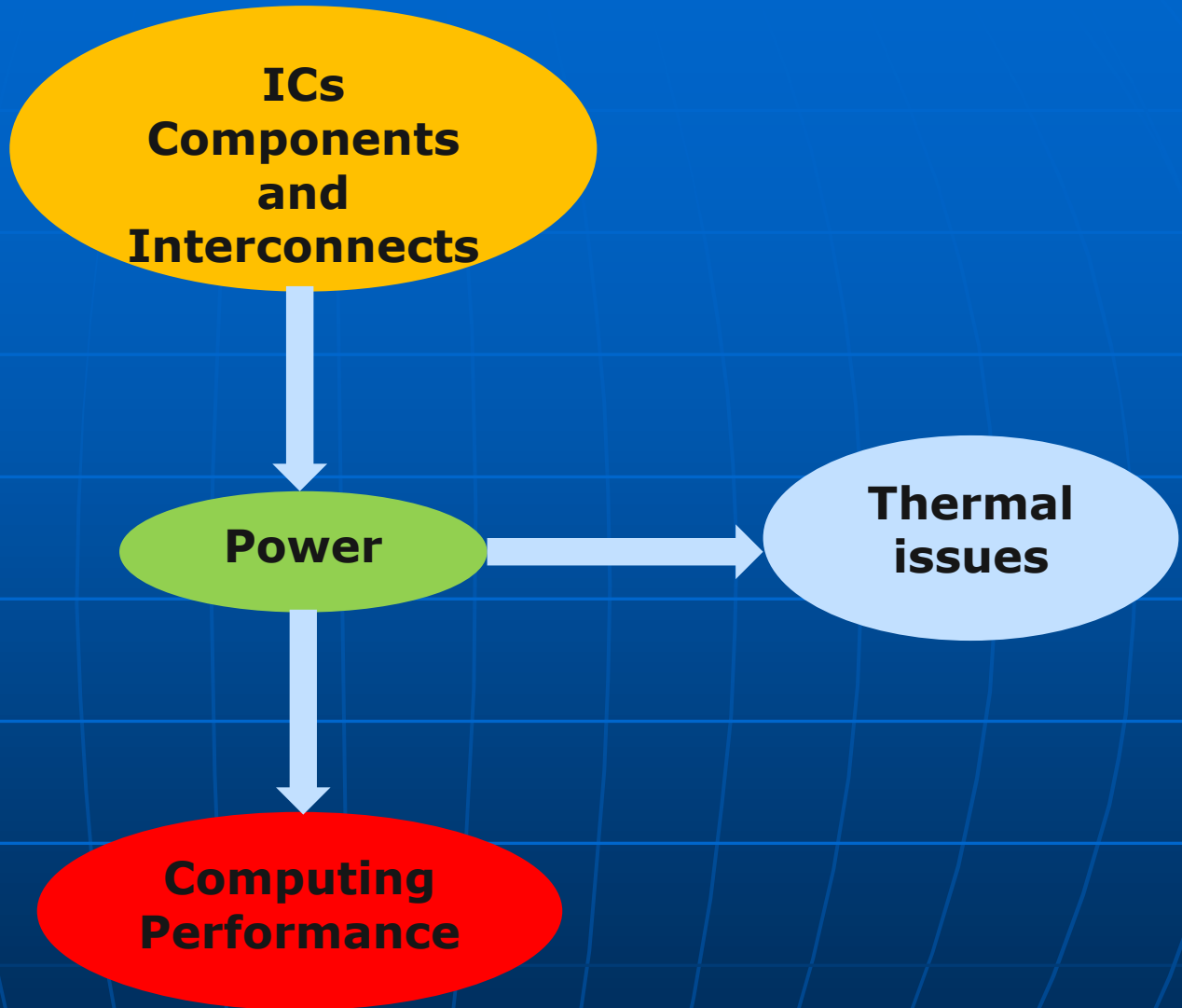
Georgia Institute of Technology, Atlanta, GA, USA

Former IBM Fellow & Director of Adv. Pkg.Tech. Lab, IBM

# Computing and Power Challenges

- Transistor Speed Slowing Down But Moore's Law Continues
- Copper Interconnects Reaching limits
  - Too Long
  - Too High a Resistance
  - Reaching Limits in Performance
- Computing Performance Continues to Escalate
  - Power Continues to Escalate
  - Thermal Continues to Escalate

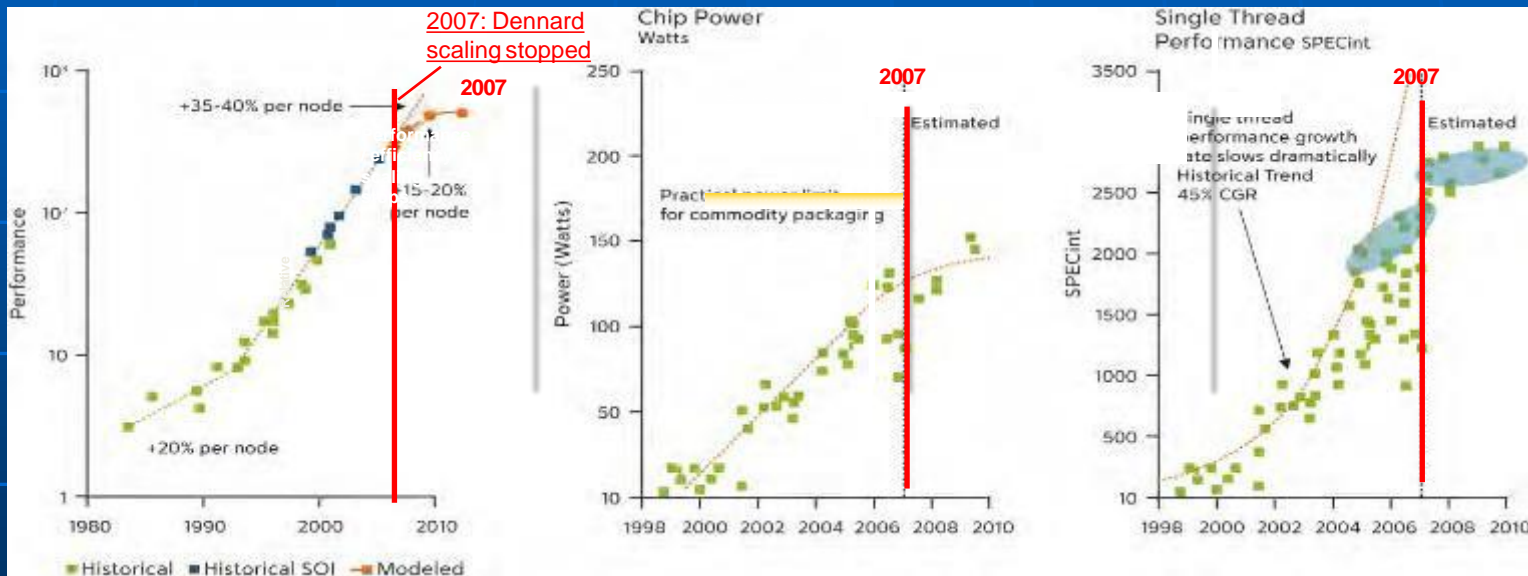
Computing by  $10^6$  X by 2040 at Same Power, Cost & Size



# Emerging Trends

- Short Term
  - Shift from SOC to SOP to improve performance
  - Shift from 2D to 3D to shorten Interconnects
  - Power chips directly or close proximity to ICs
- Mid Term
  - Optical Interconnects and Systems
  - Power Integration and minimization with Optical
- Long Term
  - Quantum Devices and Systems
- Long, Long Term
  - Human Brain

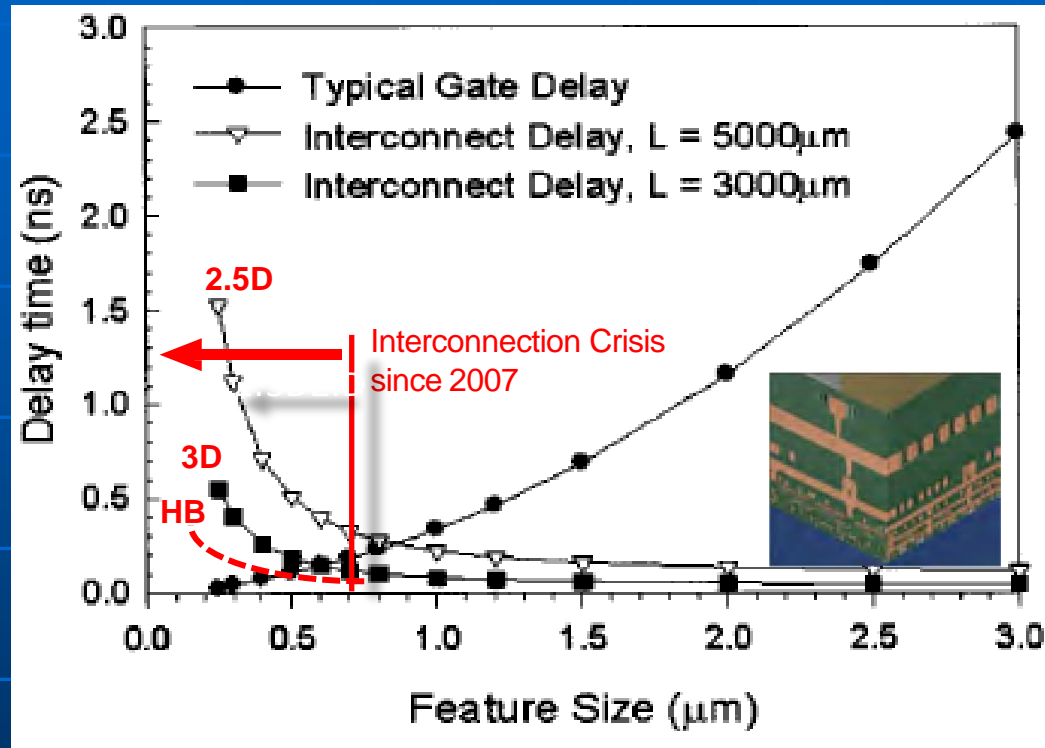
# The Limit of Traditional CMOS Transistor Scaling for Computer Performance



**Since 2006/07: Circuits still become smaller and cheaper, BUT not faster and not more efficient.**  
**Since 2016/17: Circuits still become smaller but not cheaper → Moore's economic "law" is dead**

Bruno Michel, [bmi@zurich.ibm.com](mailto:bmi@zurich.ibm.com)

# Interconnections Limiting System Performance: L, R and C



# Future Devices ?



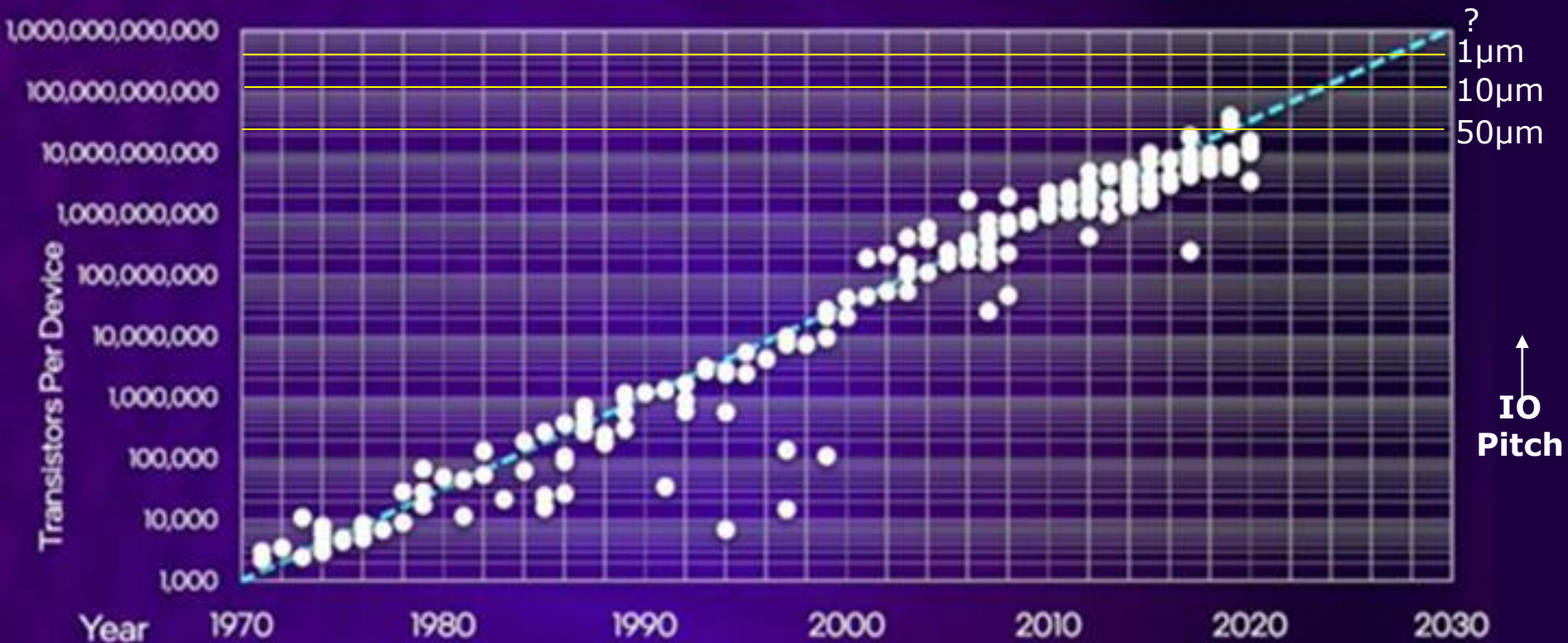
- **Non-Traditional CMOS: Ribbon Transistors**
- **Processor in Memory or Vice Versa**
- **3D SOCs**
- **Opto-electronic Devices**
- **Quantum Devices**

© Intel Corporation.

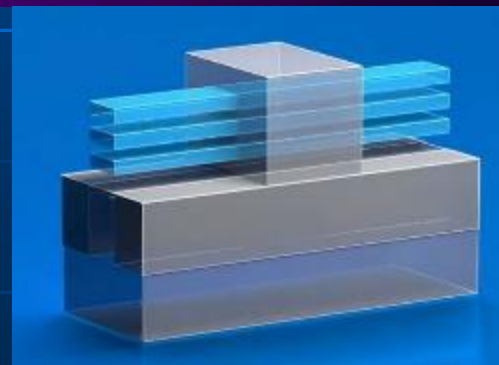
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Learn more about Intel process technologies at [www.Intel.com/ProcessInnovation](http://www.Intel.com/ProcessInnovation)  
Prof. Rao R. Tummala

# Trillion Transistor IC?



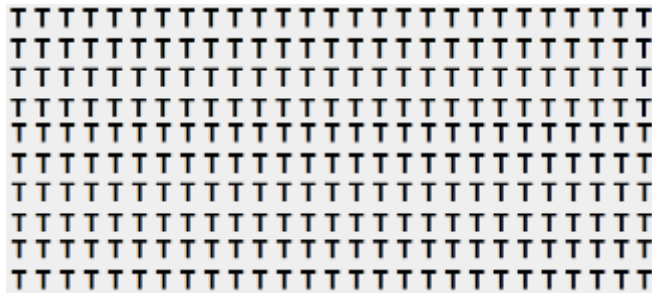
**Intel's Ribbon FET Transistor**



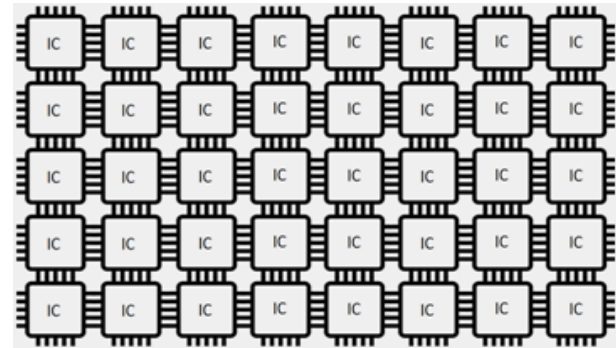


# New Moore's Law for 1 Trillion Transistors On Silicon Vs. On Package

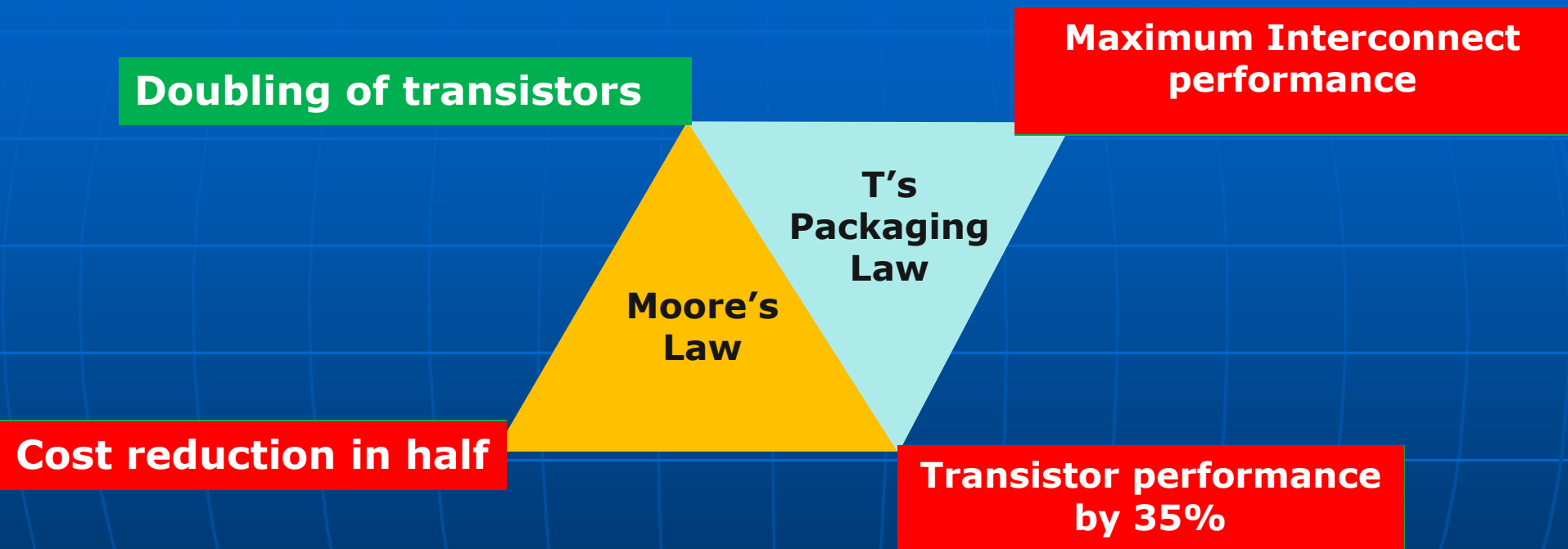
## Moore's Law for 1 Trillion transistors



## New Moore's Law for 1 Trillion



# New Moore's Law Enabled by Packaging



**Old Moore's law**

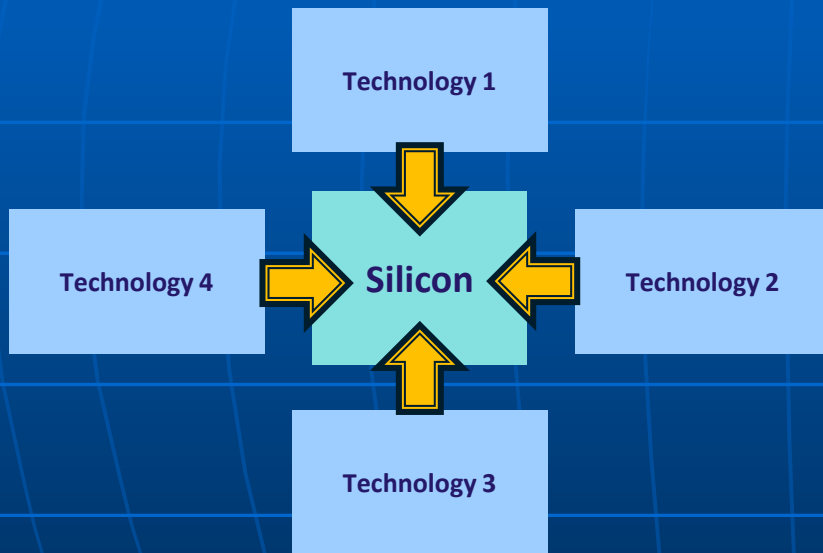


**New Moore's law: Transistors + Interconnections**

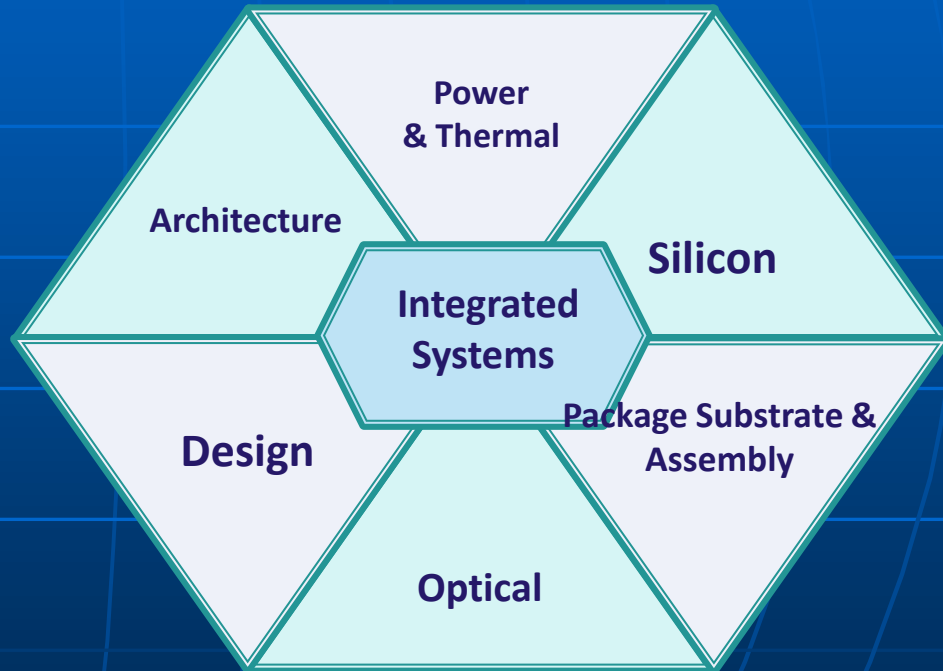
# Shift from SOC to SOP & from 2D to 3D

# Shift from SOC to SOP

Past: Value-add: Silicon



Future: Value-add by System Integration(SI)



# New Era in Packaging: Highly Integrated systems Packaging with highest Value-add

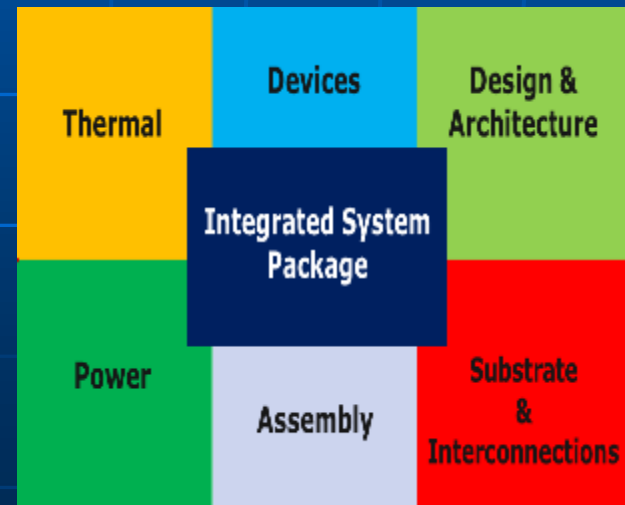
**Past**



IC Assembled on Package Substrate

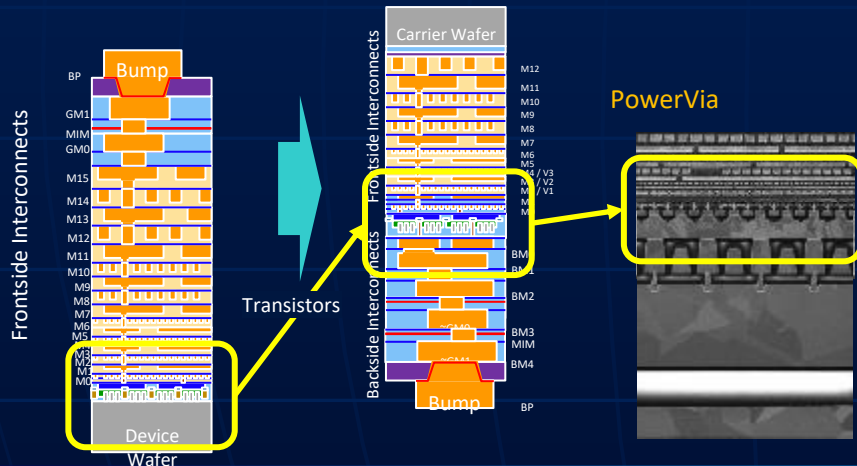
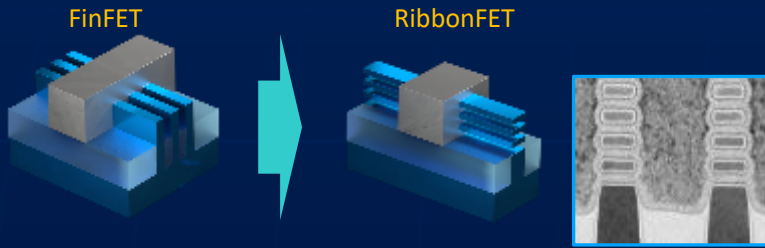
**Future**

**Integrated System Module**

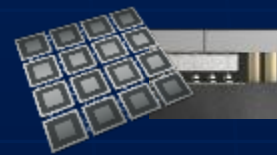


# Intel Packaging Evolution to 3D, DB & Panel Mfg.

## RibbonFET and PowerVia Technology



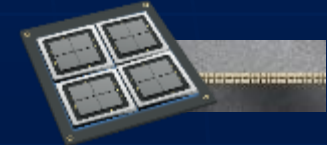
### Foveros Omni



bump pitch ~25 microns

- next gen Foveros technology
- unbounded flexibility with performance 3D stacking technology for die-to-die interconnect and modular designs

### Foveros Direct

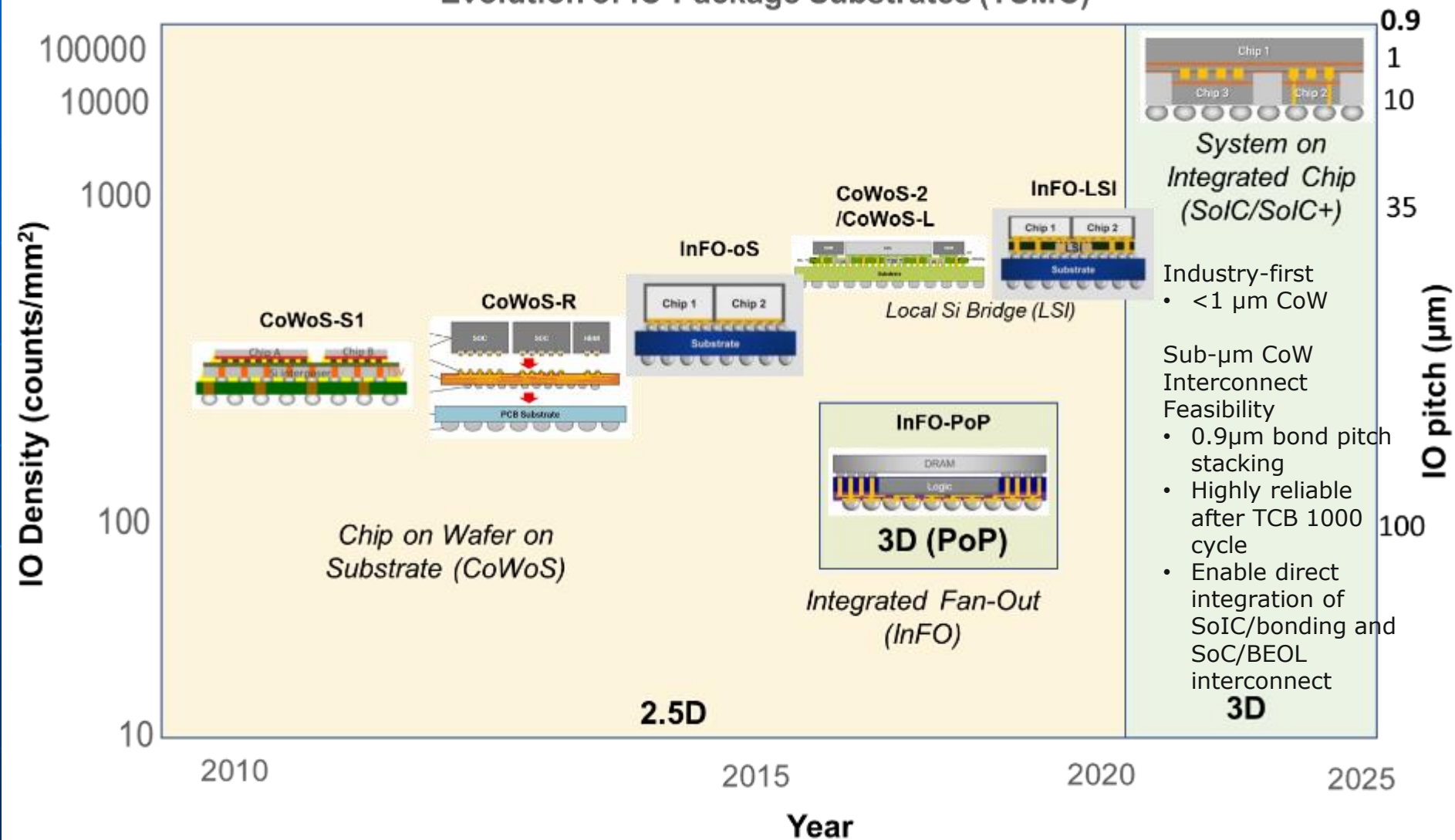


bump pitch < 10 microns

- direct copper-to-copper bonding for low resistance interconnects
- blurs the boundary between where the wafer ends and the package begins

# TSMC Packaging Evolution to 3D & HB

## Evolution of IC-Package Substrates (TSMC)

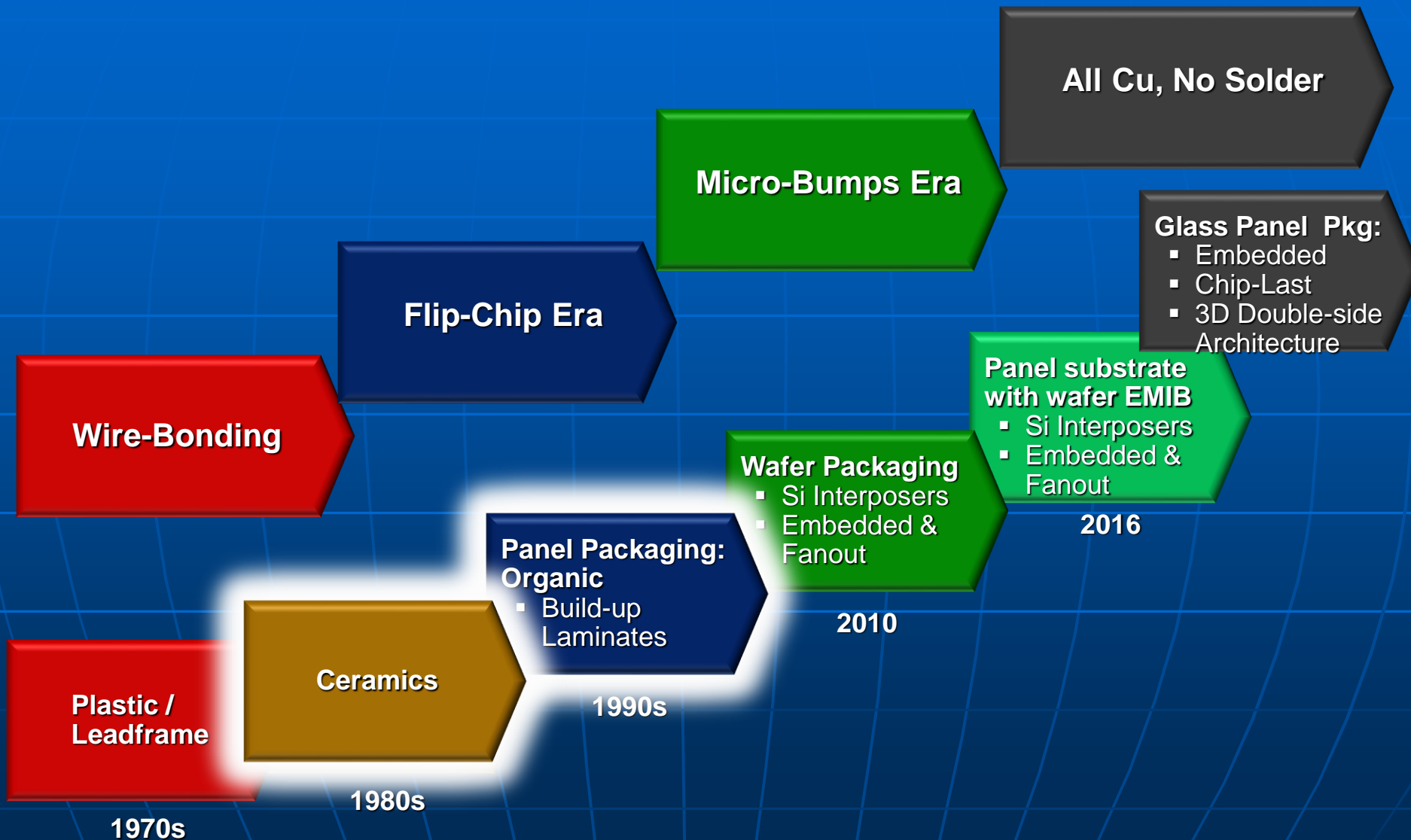


\*Scales are approximate

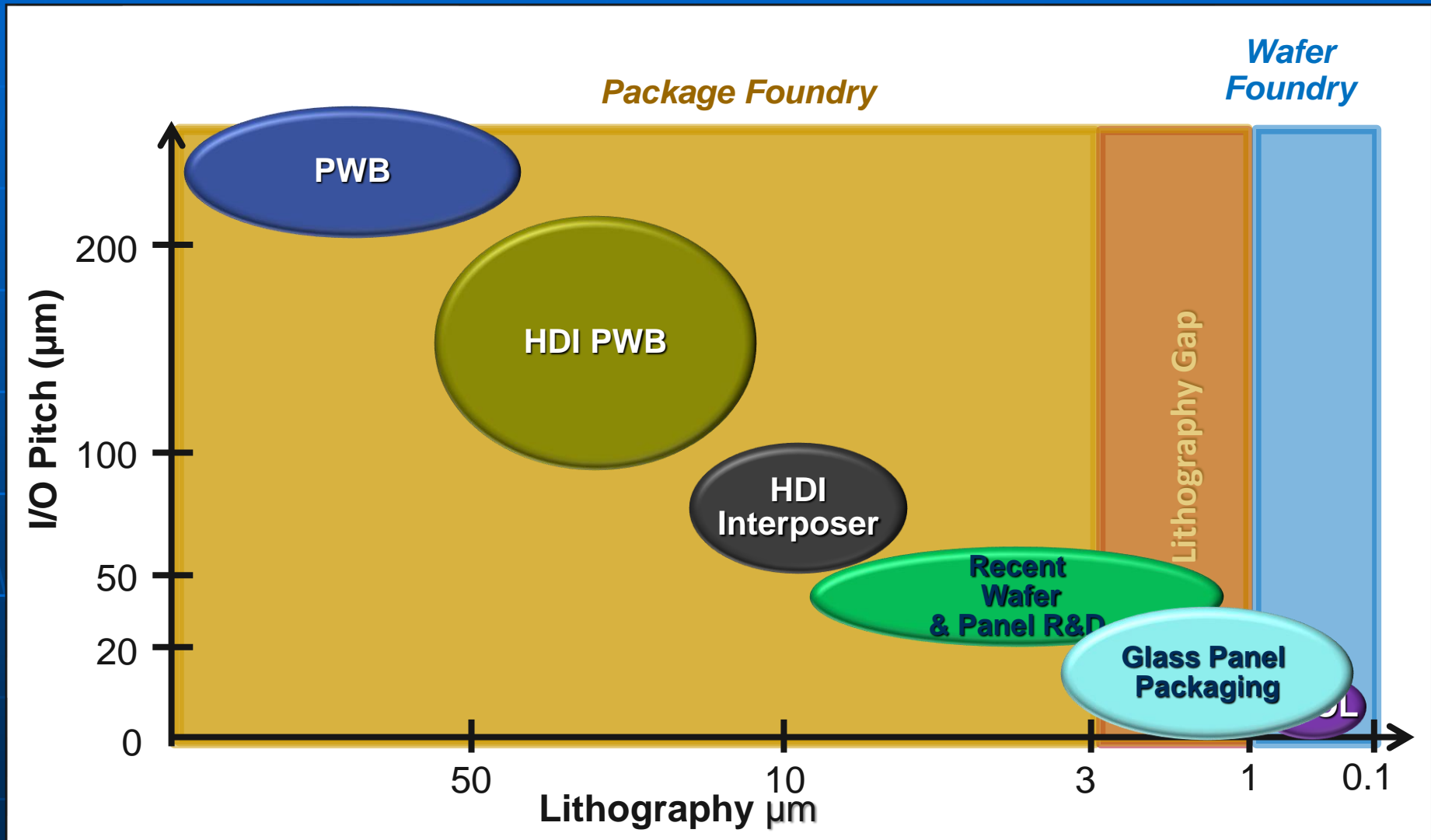
# Packaging



# Package Family Nodes in the last 6 Decades



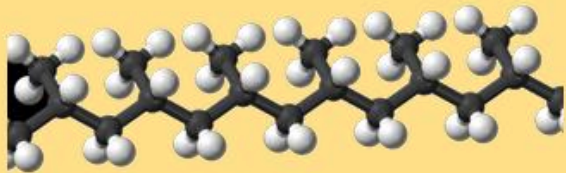
# Package Foundry Reaches Wafer Foundry Ground Rules But In Panel Size



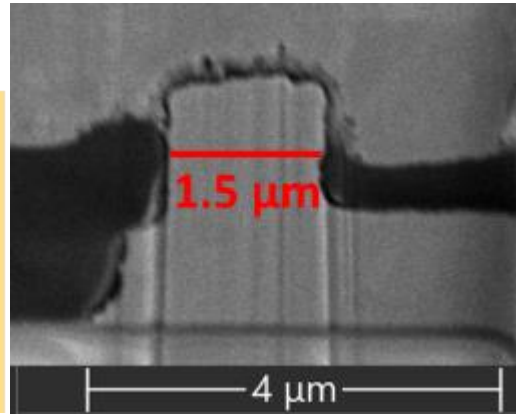
# Georgia Tech Demonstrates $<1 \mu\text{m}$ Panel RDL with Low R and C

Ultra low Dk ( $<2.5$ ) Dielectrics for low capacitance RDL

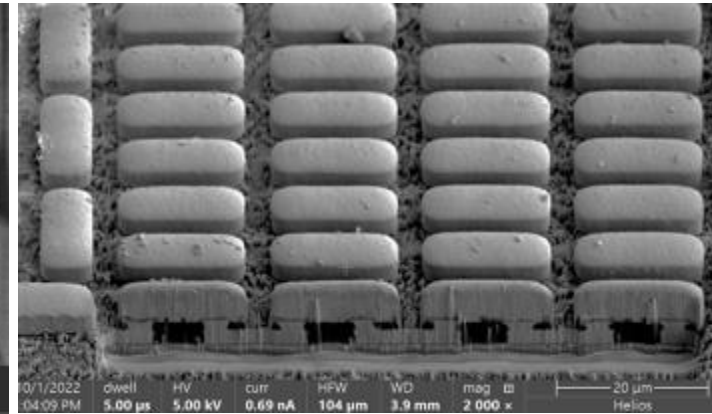
Ultra low Dk Polymers



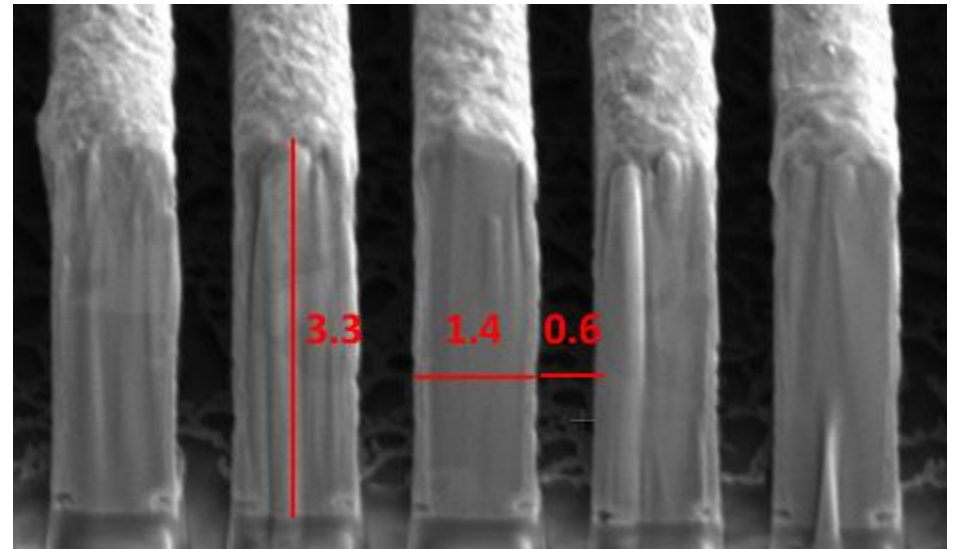
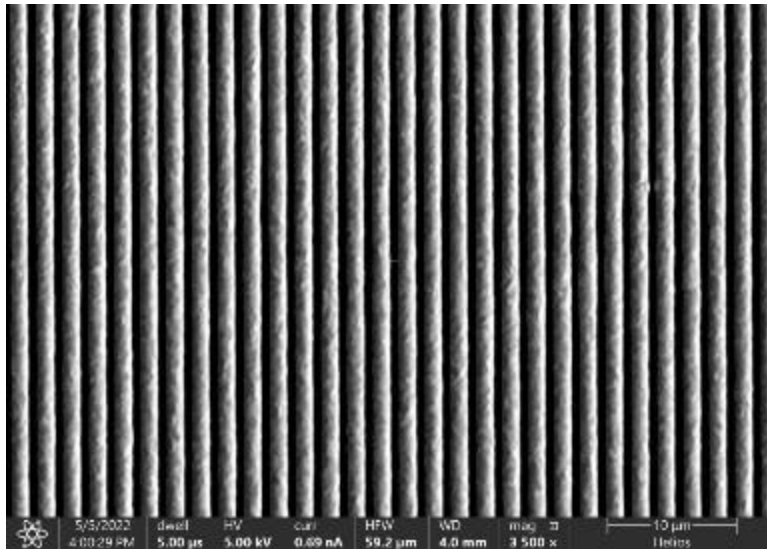
1.5 $\mu\text{m}$  Microvia



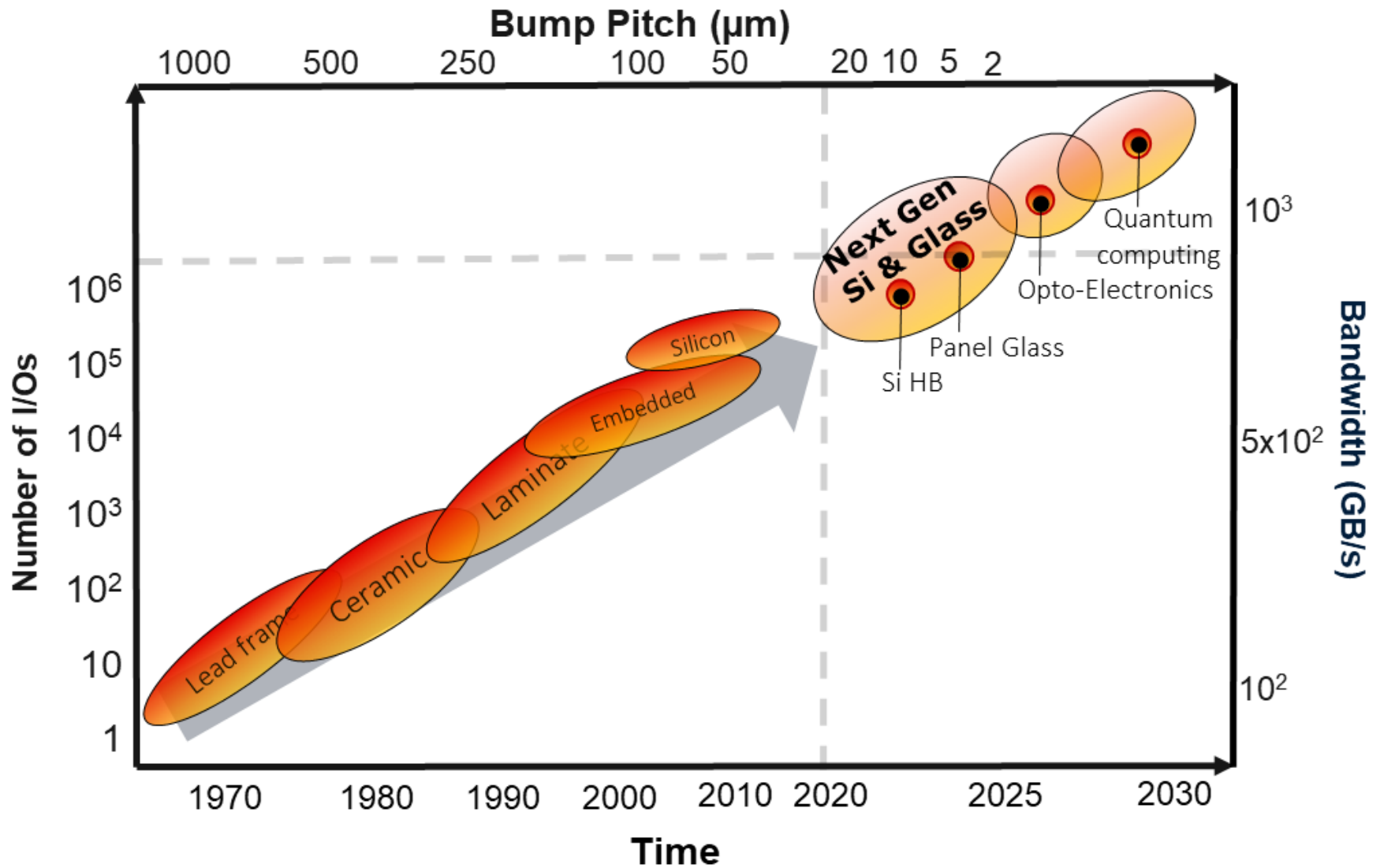
3 $\mu\text{m}$  Microvia TCT Reliability



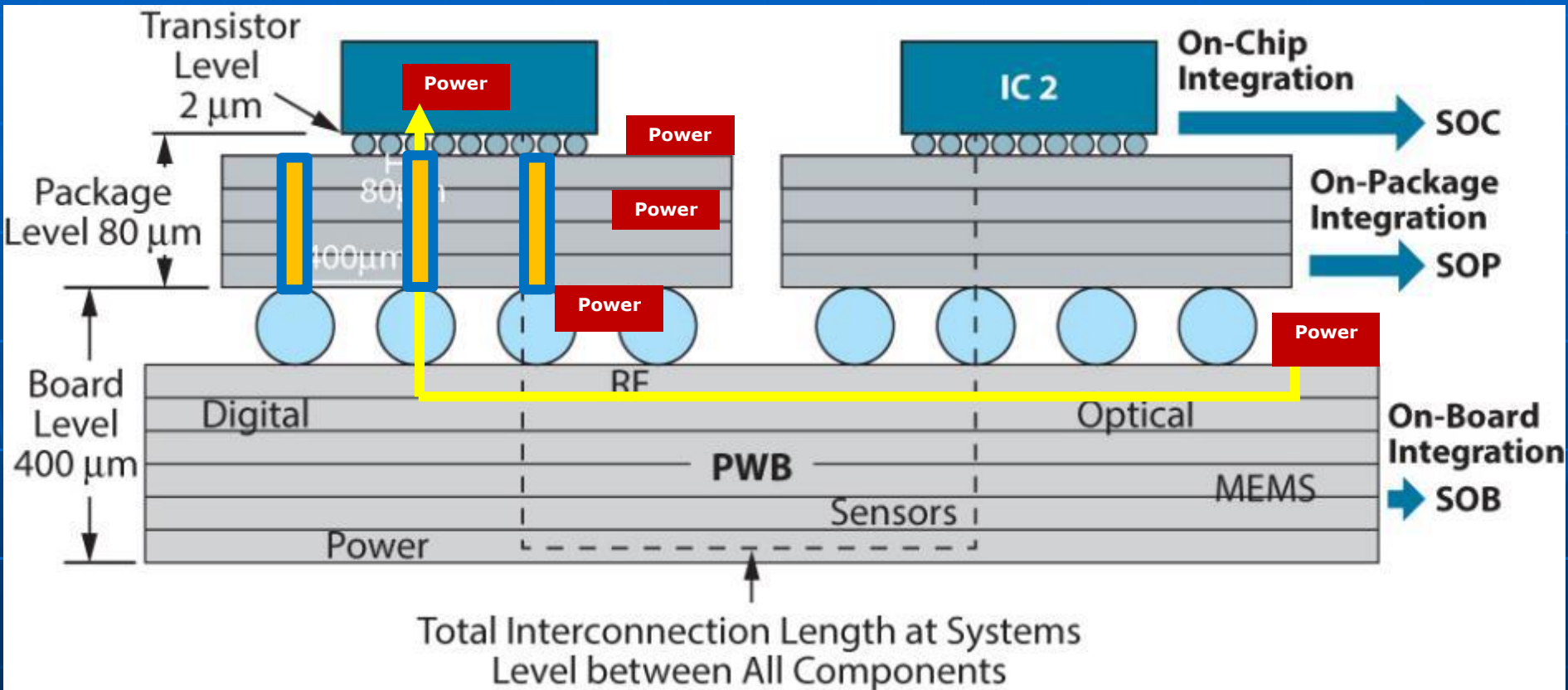
High Aspect Ratio 1 $\mu\text{m}$  RDL with novel etching process



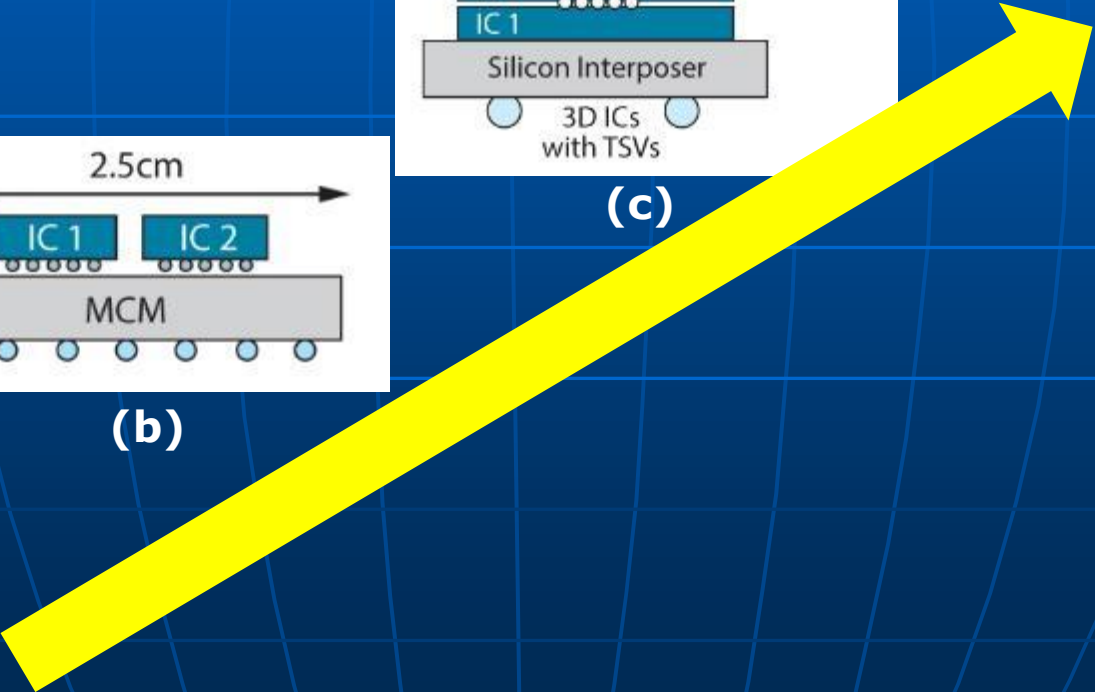
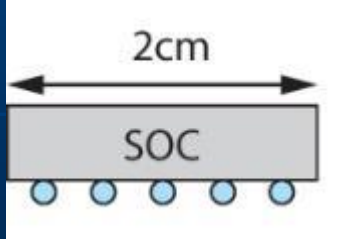
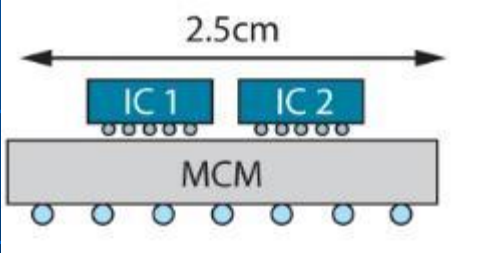
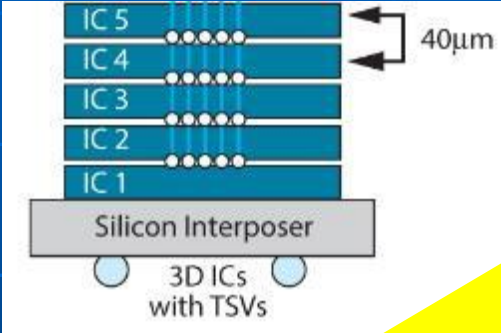
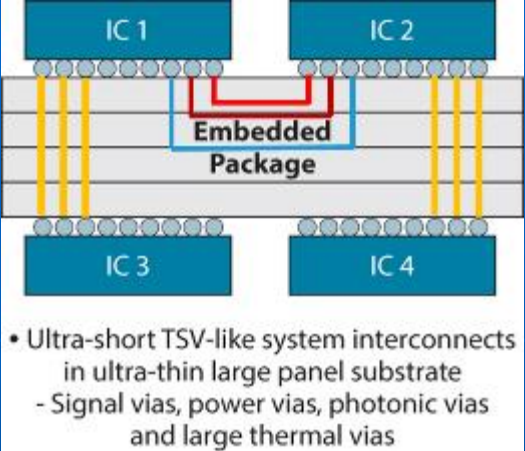
# Interconnections Evolving Just Like Moore's Law



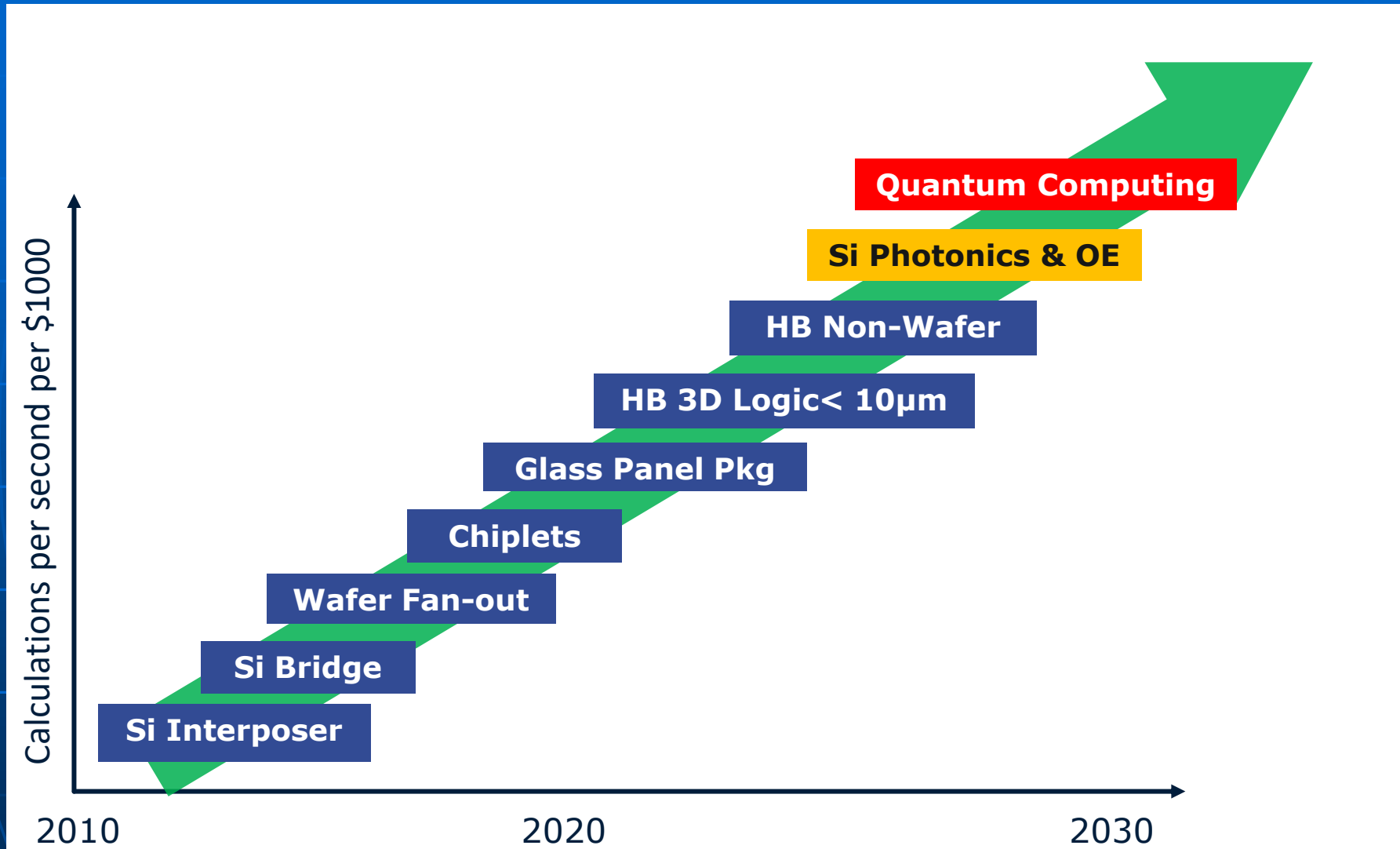
A three-level packaging hierarchy currently in use at IC, package, and board levels to form electronic systems, interconnecting all components at board level with extremely long interconnect length.



# 3D stacking of chips in contrast to: (a) SOC, (b) MCM, and (c) for interconnect length and bandwidth (d) 3D SOP double-side system architecture



# Pre- and Post- Moore's Law Electronics R&D



# Silicon Photonics and Opto-electronics

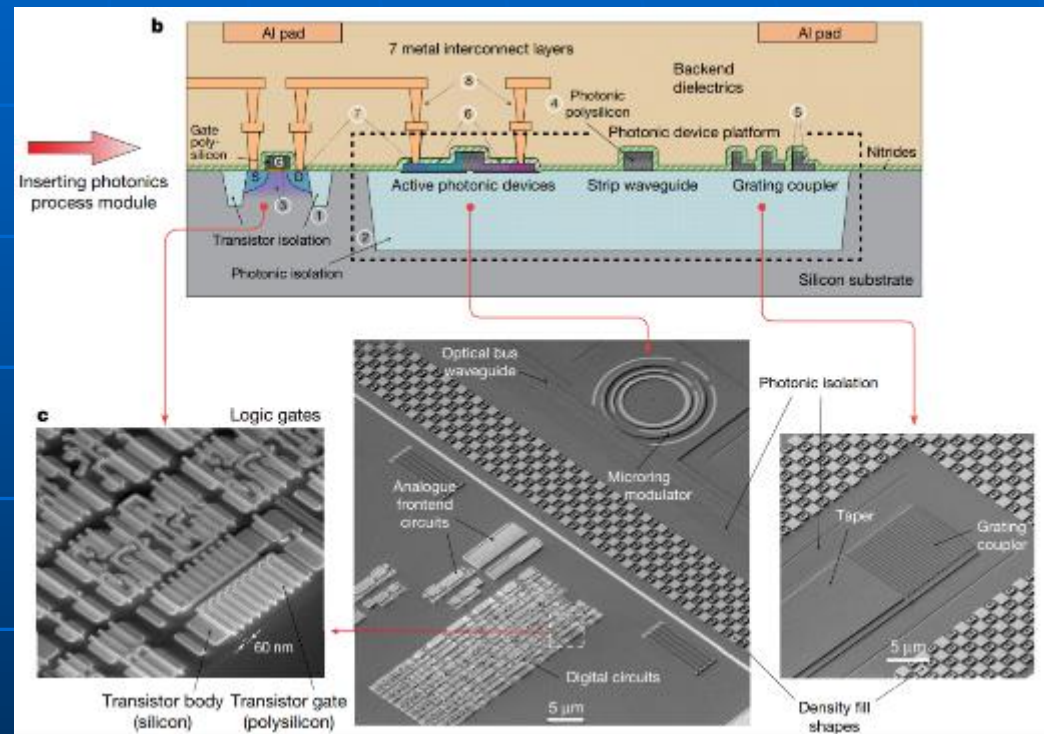
- Integrating electronic and photonic devices onto one single silicon chip using CMOS fabrication techniques.

- Advantages

- Smaller size (400 nm waveguide width)
- Mature CMOS mfg. process

- Challenges

- On-chip light sources
- Fiber integration
- Different CMOS nodes required for electronics and photonics

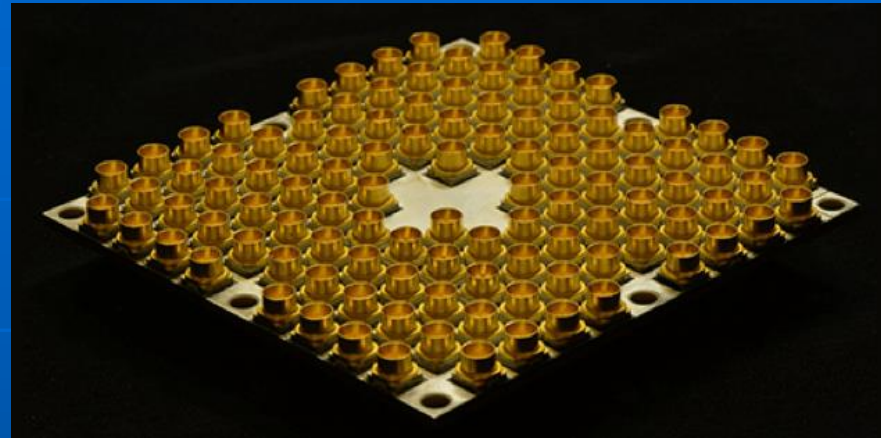


Electronic and photonic blocks on a monolithic silicon platform<sup>[1]</sup>

[1] Atabaki, A. H., Moazeni, S., Pavanello, F., Gevorgyan, H., Notaros, J., Alloatti, L., ... & Al Qubaisi, K. (2018). Integrating photonics with silicon nanoelectronics for the next generation of systems on a chip. *Nature*, 556(7701), 349.



Intel's 49-qubit quantum Tangle Lake processor, including 108 RF gold connectors for microwave signals. Source: Intel

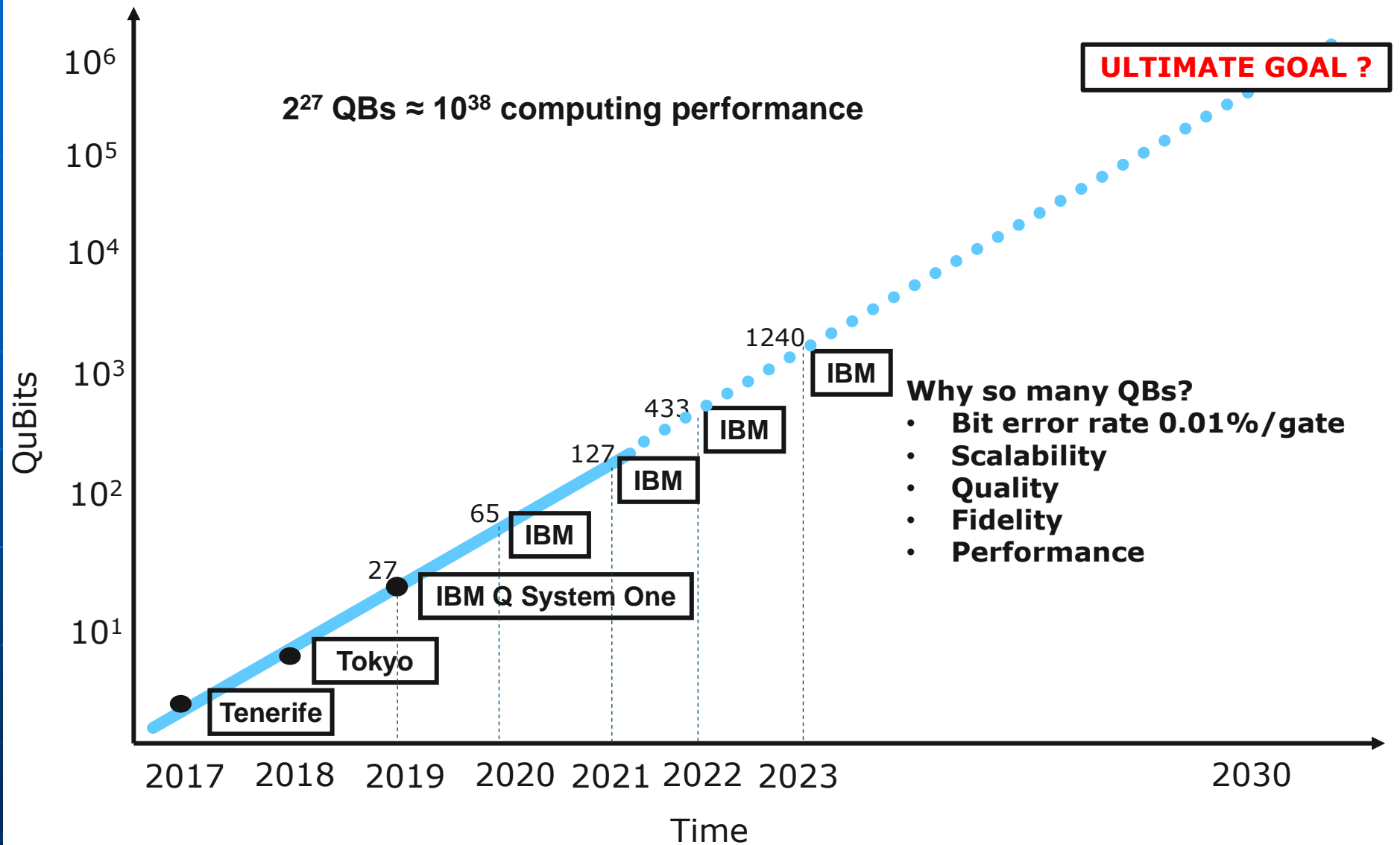


D-Wave's quantum chips. Source: D-Wave



IBM's 127 QB quantum computer system. Source: IBM





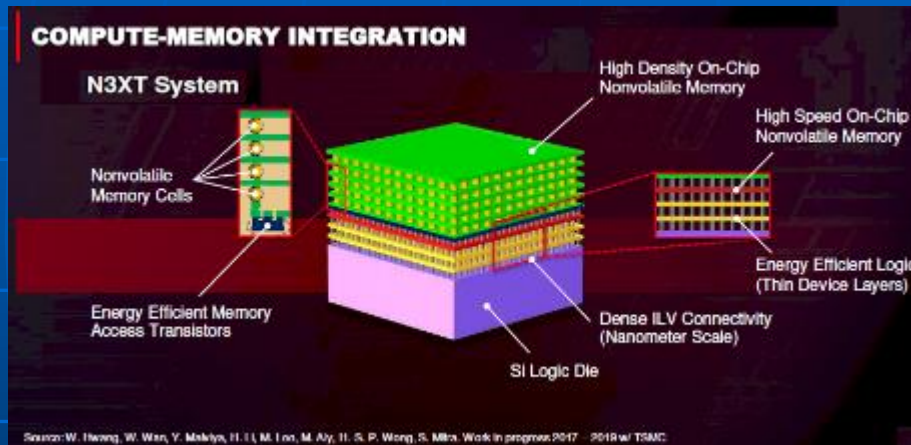
# Grand Challenges In Engineering by NAE, USA

1. Make solar energy economical
2. Provide energy from fusion
3. Develop carbon sequestration methods
4. Manage the nitrogen cycle
5. Provide access to clean water
6. Restore and improve urban infrastructure
7. Advance health informatics
- 9. Reverse-engineer the human brain**
10. Prevent nuclear terror
11. Secure cyberspace
12. Enhance virtual reality
13. Advance Personalized learning
14. Engineer the tools of scientific discovery

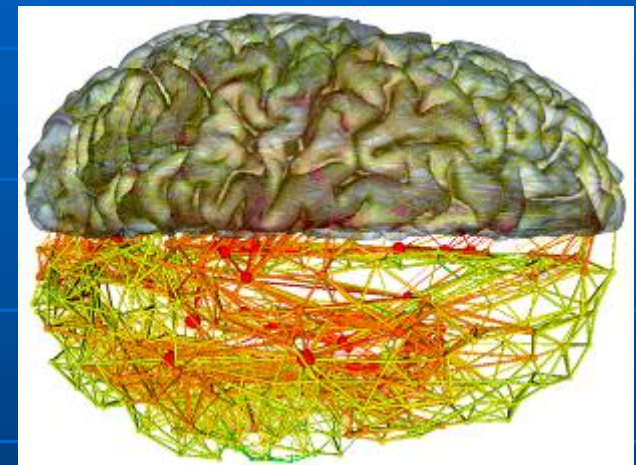


NATIONAL ACADEMY OF ENGINEERING

# Electronics are Planar and 3D, Unlike Human Brain with Billions of Interconnections in > 3D



3D Electronics

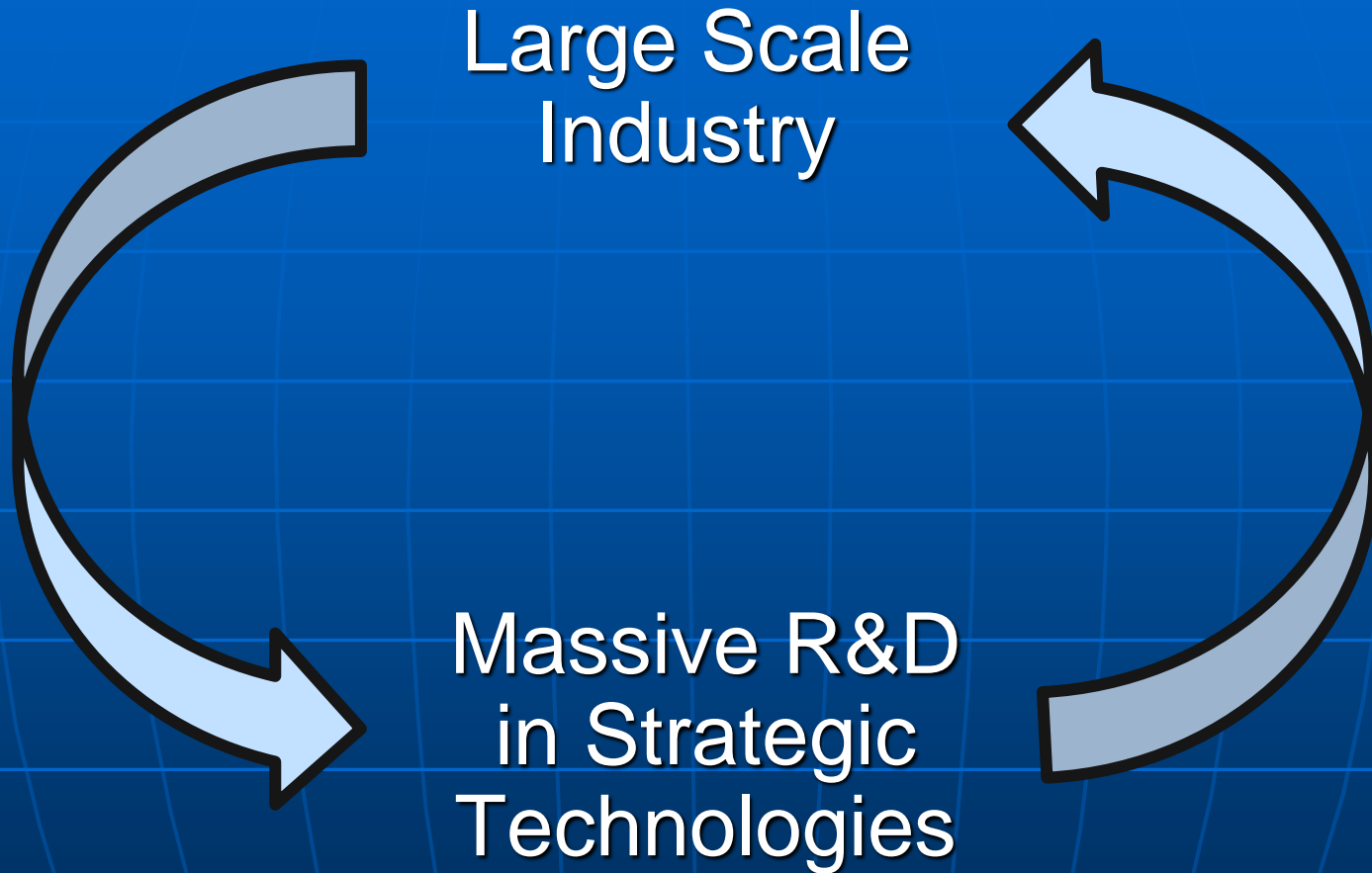


5D Human Brain

# Emergence of India in Electronics

- US-India announce to set up a private-sector taskforce to identify
  - Near Term Mfg. Opportunities including chip mfg.
  - Long Term Strategic Opportunities
    - R&D
    - Workforce
    - Exchange

# India Needs Large Scale Electronics Industry



# Emergence of India as A Manufacturing Country

- Plans to be 3<sup>rd</sup> Largest Economy by 2030
- Fastest Growing G20 Economy
- 2nd Largest Internet User
- 3<sup>rd</sup> Largest Start- up System
- 33M Graduates
  
- Announced ISM Agency and \$10B Incentives for:
  - ICs
  - Packaging
  - Displays

# India's strengths and Weaknesses in Electronics

## Competitiveness of India in Electronics

	India
Market size	Strong
Educated workforce in Basic Sciences & Eng.	Strong
Educated workforce Design	Strong
Educated workforce in R&D Technologies	Weak
Educate workforce in Manufacturing	Weak
Market size and Investment opportunities	Strong

Strong Fair Weak

Prof. Rao R. Tummala



# India to Transform from Design-centric to System-centric

## Current: Design-centric

- IC & Package Design
- Software



## Vision: System-centric

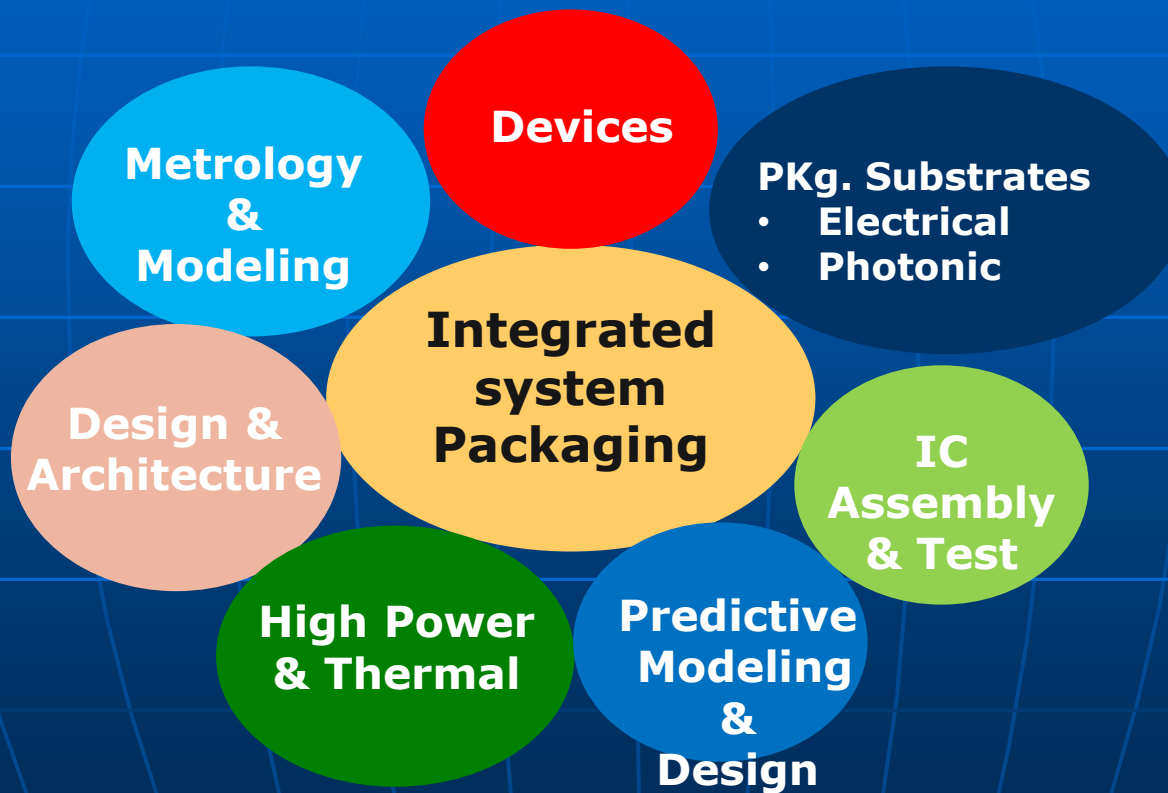
- System Design
- System-level software
  - Multinational
  - Domestic
- System technologies
  - Devices
  - On-chip packaging
  - Substrates: RF, O-E
  - Components
  - Interconnections
  - Design & Architecture
  - Power
  - Thermal
  - Assembly
  - Test

## End Goal:

### Integrated systems & Products for

- Domestic Market
- Export market

# R&D Areas



# Emergence of R&D in Semiconductors, Packaging and Systems in India

- **12 Premier Institutes from India**
  - IIT Bombay
  - IIT Jodhpur
  - IIT Kanpur
  - IIT Madras
  - IIT Roorkee
  - IIT Delhi
  - IIT Kharagpur
  - IIT Gandhinagar
  - IIT Guwahati
  - IIT Hyderabad
  - IIT Ropar
- **100+ Interdisciplinary Faculty in Electrical, Materials, Chemical, Mechanical, Chemistry, Physics, ...)**



Participating Institutes

# Industry Partners in R&D & Mfg.

- **\$10B Incentives in ICs, Packaging, Displays**

**Automotive**

**Compound  
Semiconduc  
tors  
& High  
Power  
Modules**

**Computing  
and AI**

**6G &  
Beyond**

**Sensing  
Electronics**

# Summary

- Device & Packaging Technologies Reaching limits in R&D
- Integrated Systems Pkg. is Strategic & High value add
- Power integration from design to system integration is critical
- Need system technologies and their integration for dramatically-improved performance at dramatically reduced power