VIRGINIA TECH

CPES
Center for Power Electronics Systems

Substrate Technologies for Medium-Voltage Silicon Carbide Power Modules

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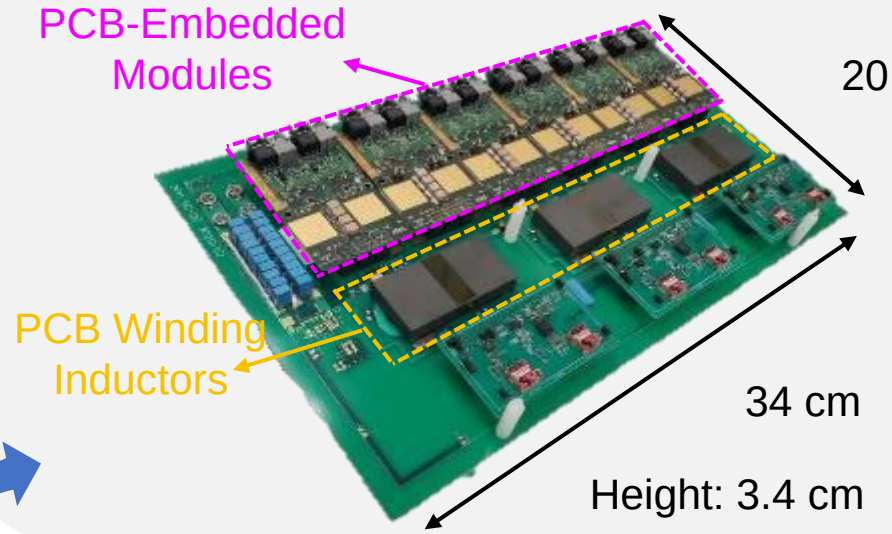
Outline

- Background
- PCB Embedding – 1.2 kV SiC half-bridge for EV on-board charger
- Organic Substrates / IMS – 1.7 kV SiC PEBB for shipboard system
- Stacked Ceramic Substrates – 10 kV SiC half-bridge for grid
- Conclusions

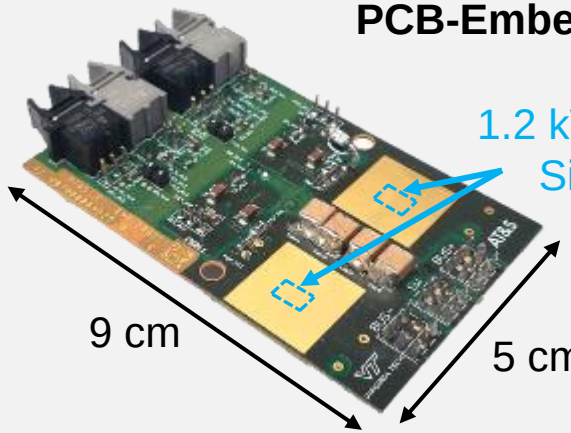
PCB-Embedded SiC Module with Double-Sided Cooling

22 kW Three-Phase AC/DC Converter



- ✓**98.2%** peak efficiency
- ✓**9.8 kW/l** power density

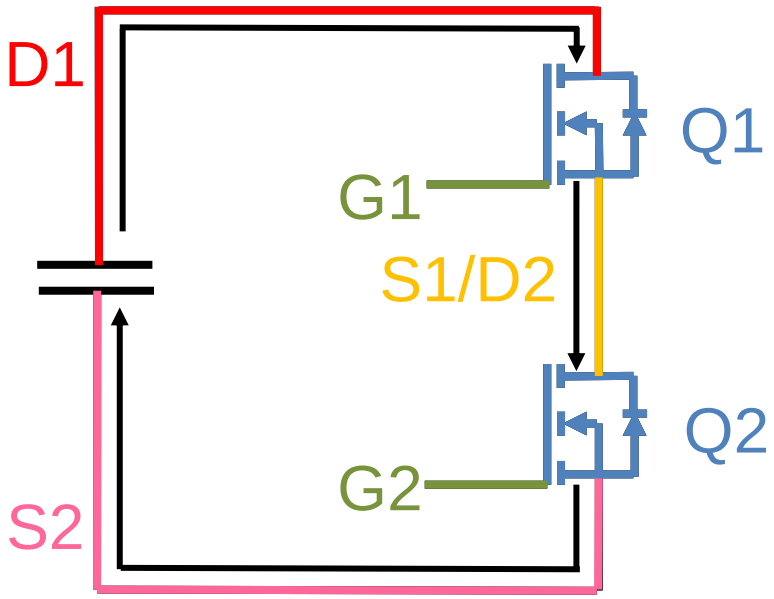
PCB-Embedded 1.2 kV SiC MOSFET Half-Bridge Module

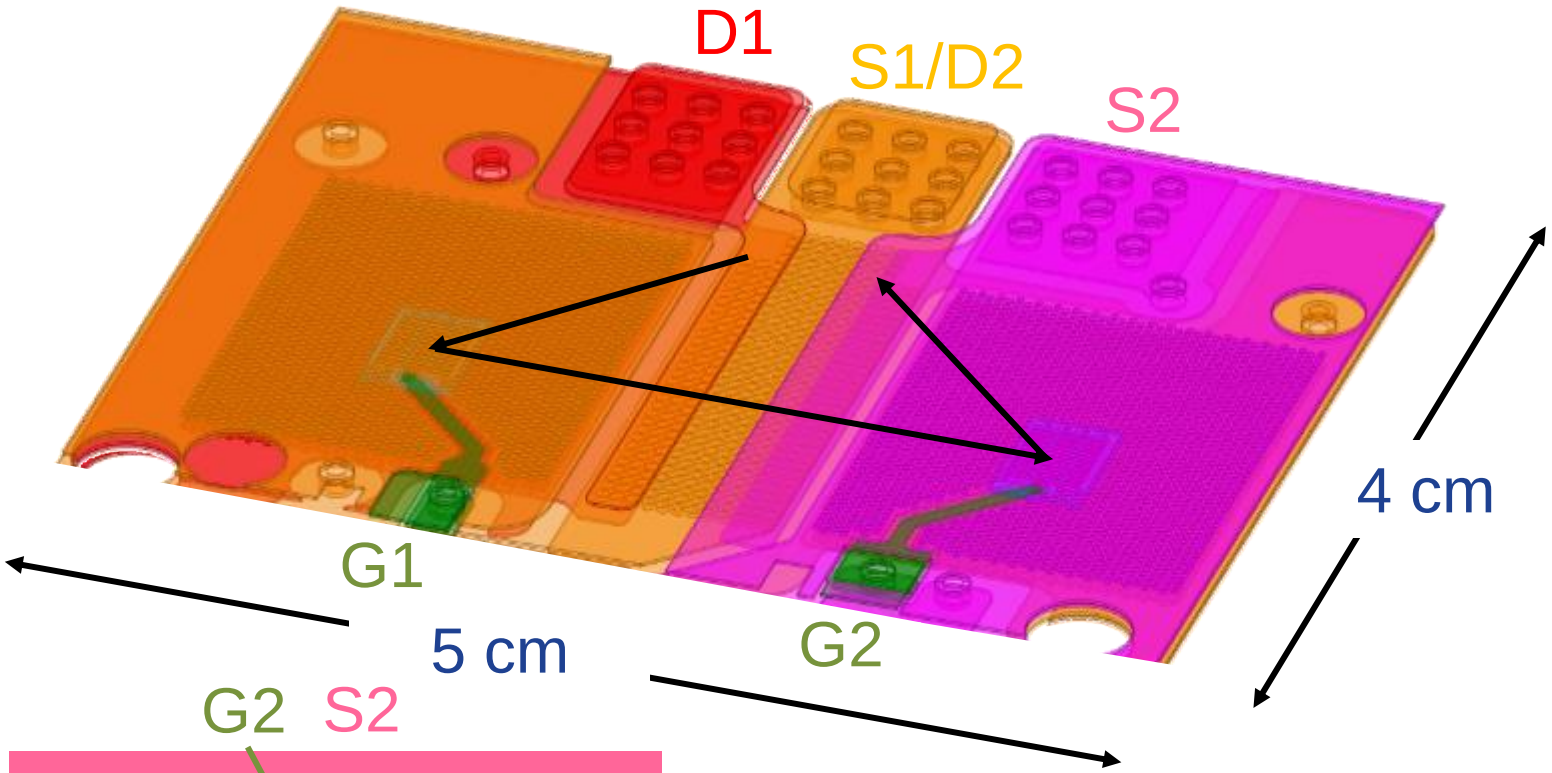


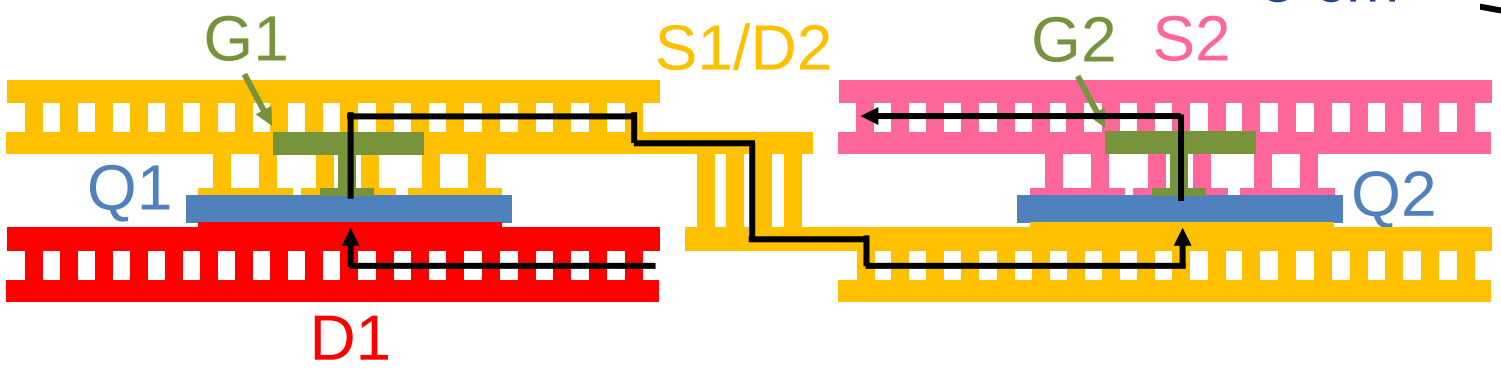
- ✓ **2 nH** stray inductance
- ✓ **1 %** voltage overshoot
- ✓ **0.12 K/W** junction-to-case thermal resistance
- ✓ **0.1 cm** height

J. Knoll et al., ECCE, 2021, doi: 10.1109/ECCE47101.2021.9596034.
J. Knoll et al., IEEE TPEL, doi: 10.1109/TPEL.2022.3177369.

PCB-Embedded Half-Bridge Design



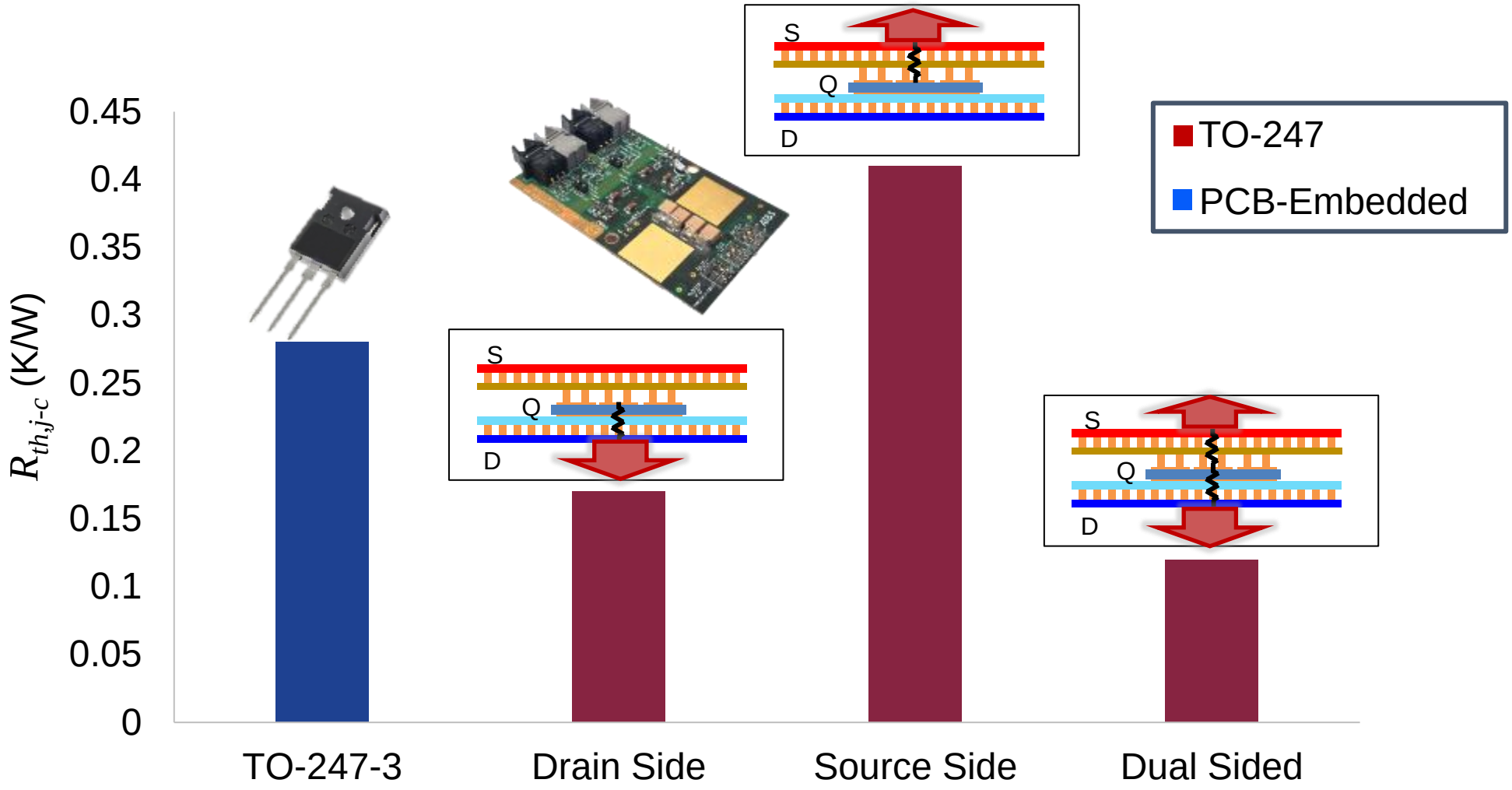




- ✓ 2 nH stray inductance
- ✓ Double-sided cooling

J. Knoll et al., ECCE, 2021, doi: 10.1109/ECCE47101.2021.9596034.
J. Knoll et al., IEEE TPEL, doi: 10.1109/TPEL.2022.3177369.

Experimental Thermal Resistance Measurements

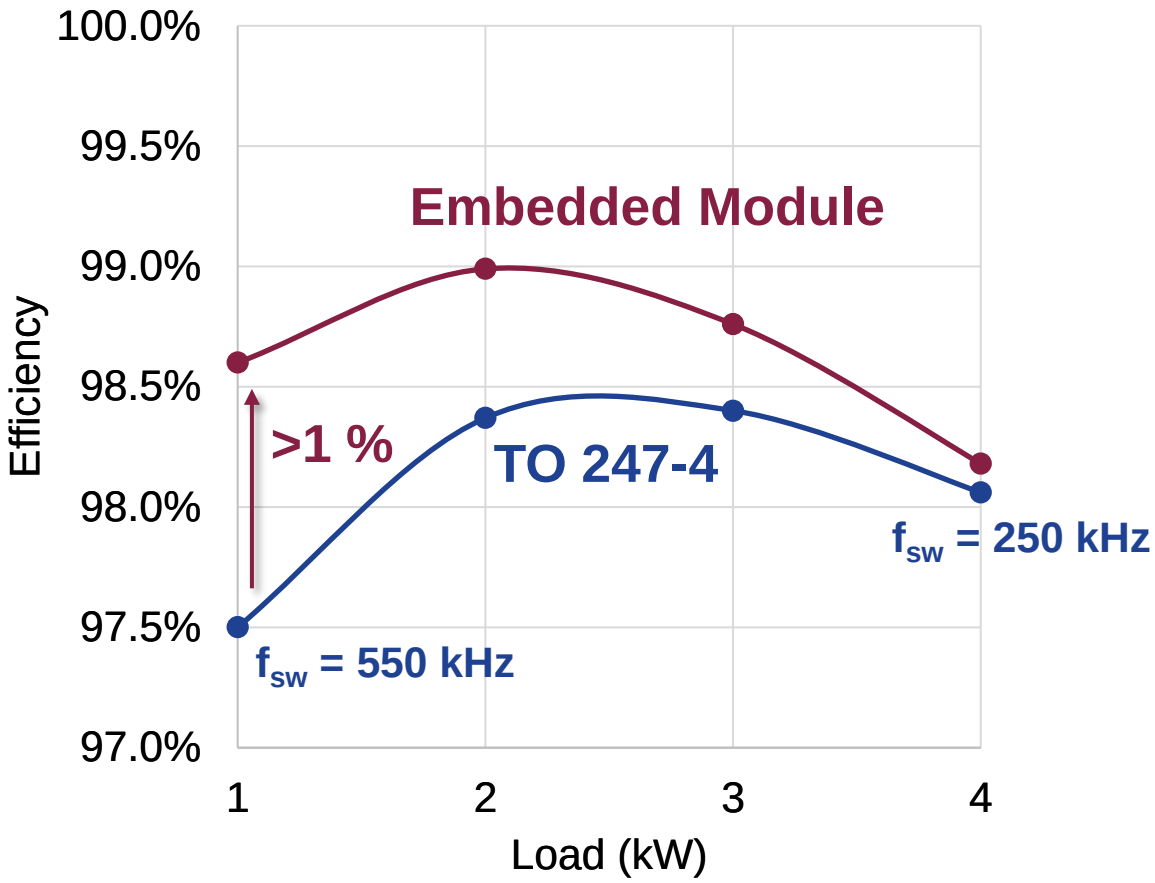


➢ **57%** lower R_{th} than TO-247

J. Knoll et al., ECCE 2022, doi: 10.1109/ECCE50734.2022.9947814.
J. Knoll et al., IEEE TPEL, doi: 10.1109/TPEL.2022.3177369.

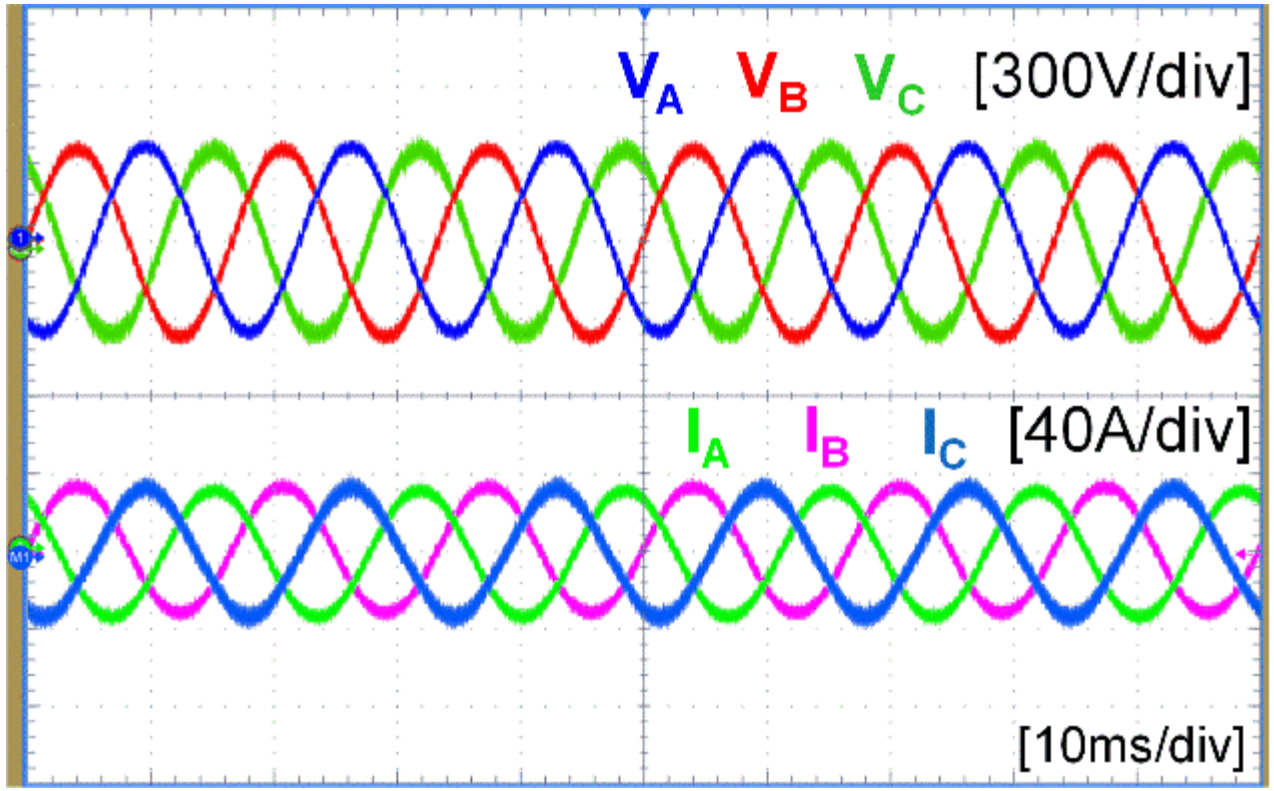
Efficiency Measurements & 3-Phase Converter Testing

CRM Boost Efficiency Comparison



22 kW AC-DC Converter Waveforms

V_{AC} = 480 VLL, V_{DC} = 800 V, P = 22 kW, f_{SW} = >300 kHz

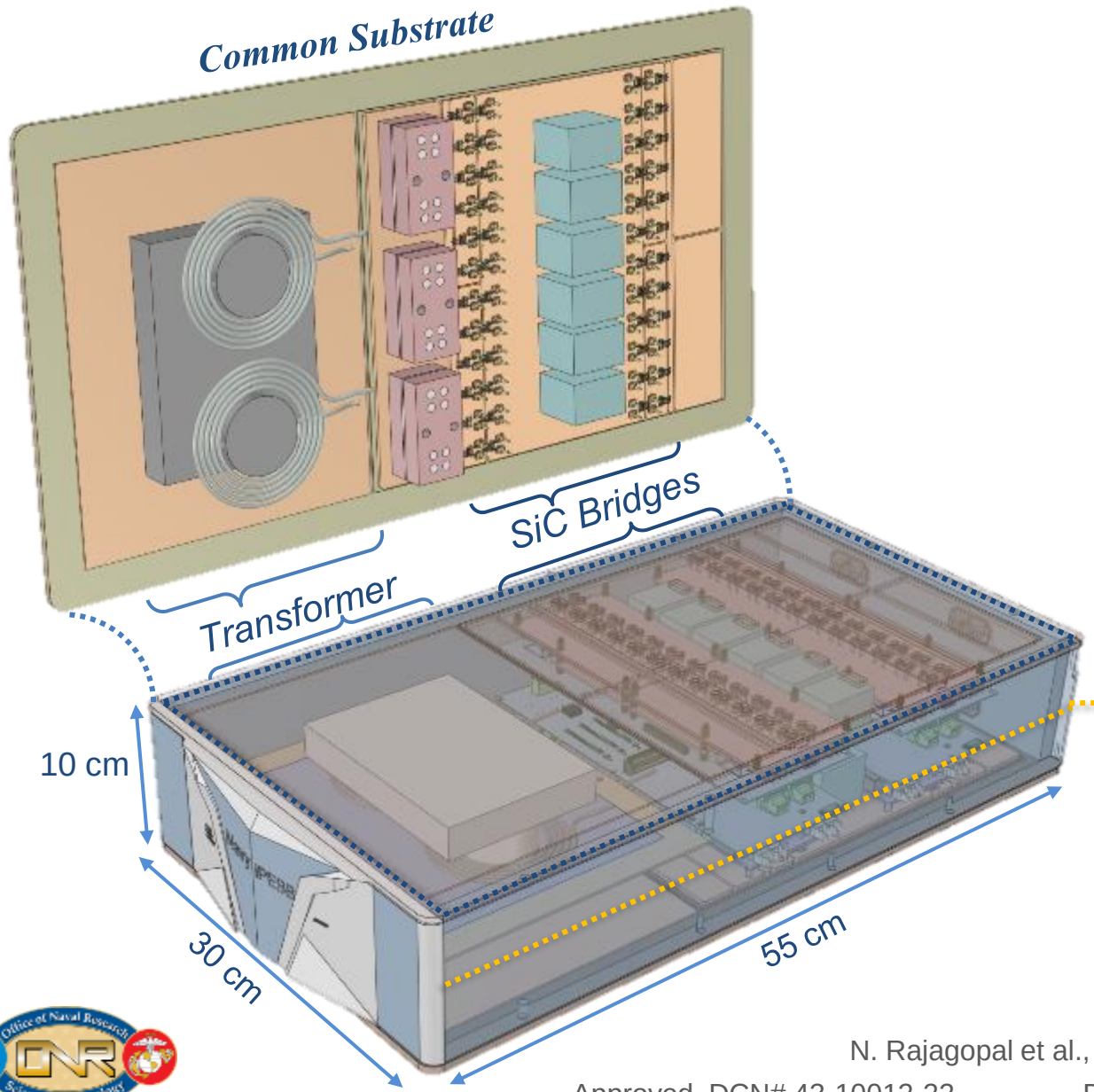


- **1%** higher efficiency at light load
- **98.2%** efficiency at 22 kW

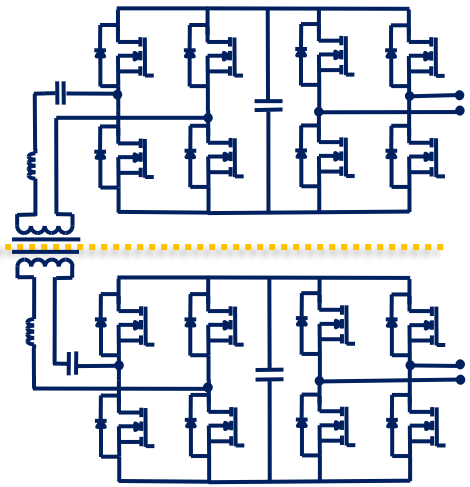
AT&S

J. Knoll et al., ECCE, 2021, doi: 10.1109/ECCE47101.2021.9596034.
J. Knoll et al., IEEE TPEL, doi: 10.1109/TPEL.2022.3177369.

Integrated Power Electronics Building Block (iPEBB)



Parameter	Target
Voltage	1 kV dc
Power	250 kW
Switching Frequency	500 kHz
Power Density	15 kW/l
Weight	35 lbs



Other Requirements

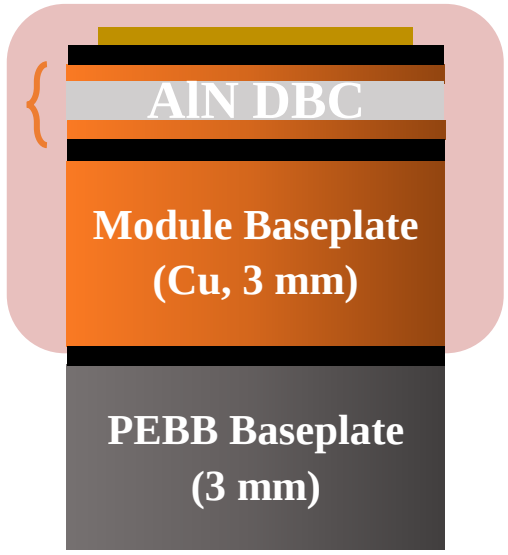
- Galvanic isolation
- AC-DC, DC-AC, DC-DC
- Bidirectional
- High manufacturability
- No liquid cooling inside PEBB

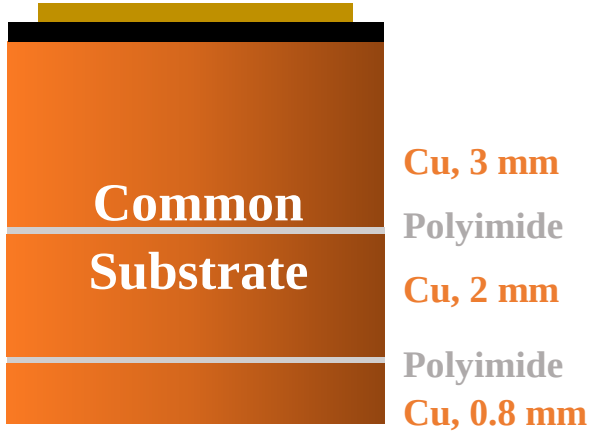
N. Rajagopal et al., IEEE APEC, 2021, doi: 10.1109/APEC42165.2021.9487167

Common Substrate Concept

Commercial Module

Navy iPEBB





= *1.7 kV SiC MOSFET die*

= *Interface layer (solder, thermal grease)*

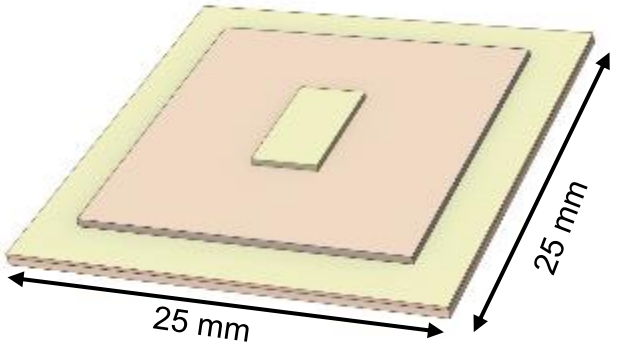
= *Copper (Cu)*

= *Aluminum (Al)*

The ODBC serves as the:

- DBC substrate
- Heat spreader
- PEBB bus bar
- PEBB baseplate

ODBC Thermal Challenge

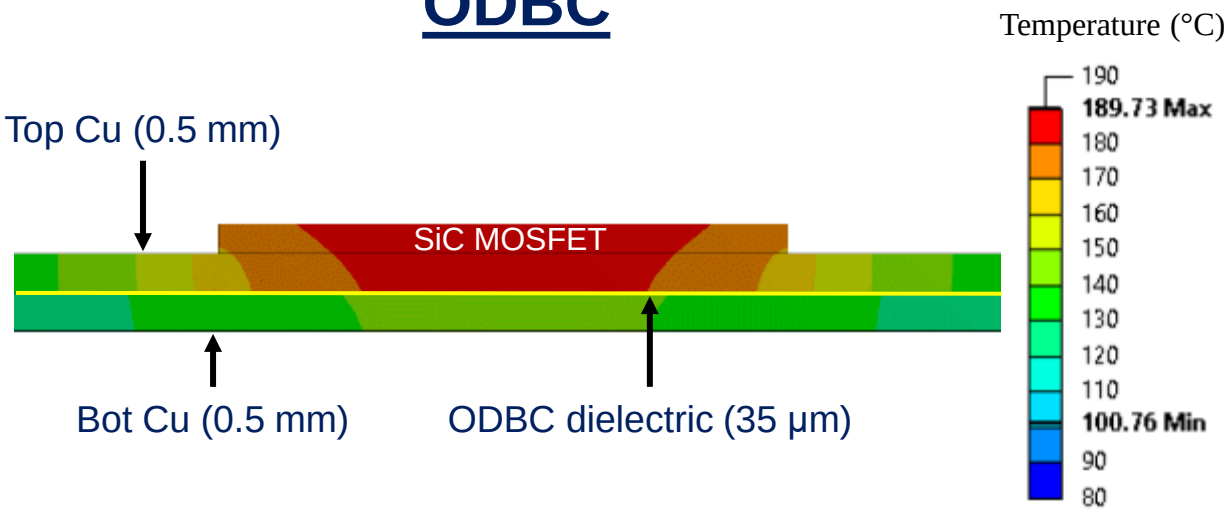


Simulation Setup

Loss: 100 W

Cooling: 3000 W/m^{2}K

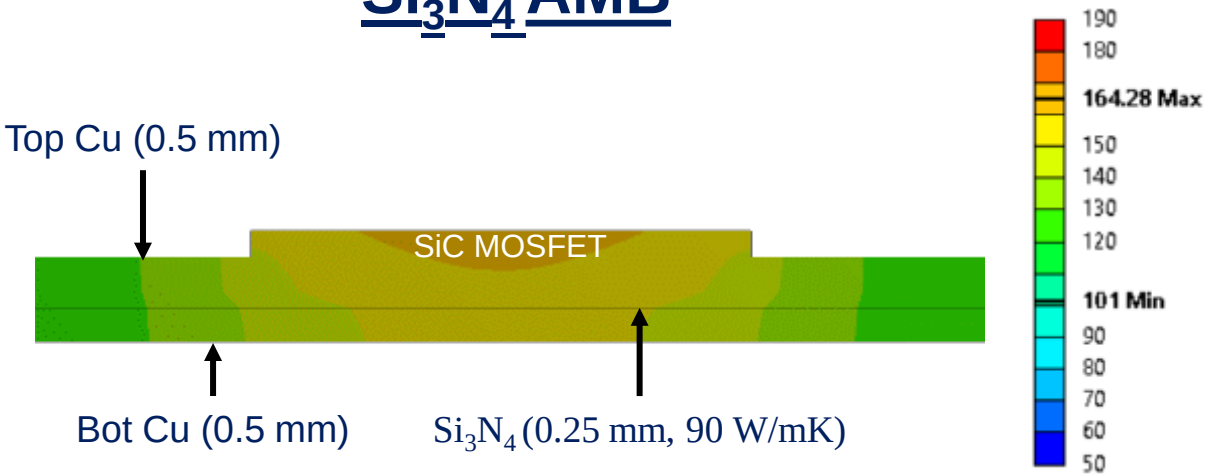
ODBC



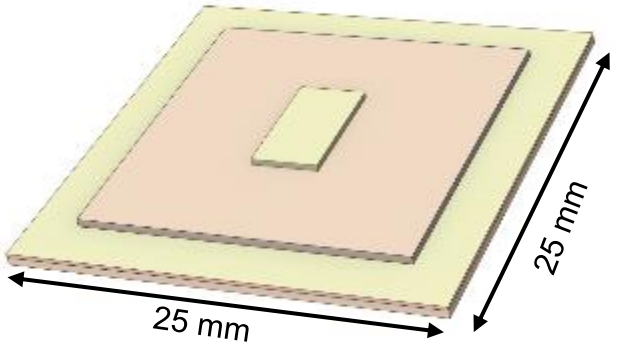
Can reduce thermal resistance by:

- Minimizing dielectric thickness
- Increasing top metal thickness
- Maximizing metal area
- Integrating cooler

Si_3N_4 AMB



ODBC Thermal Challenge



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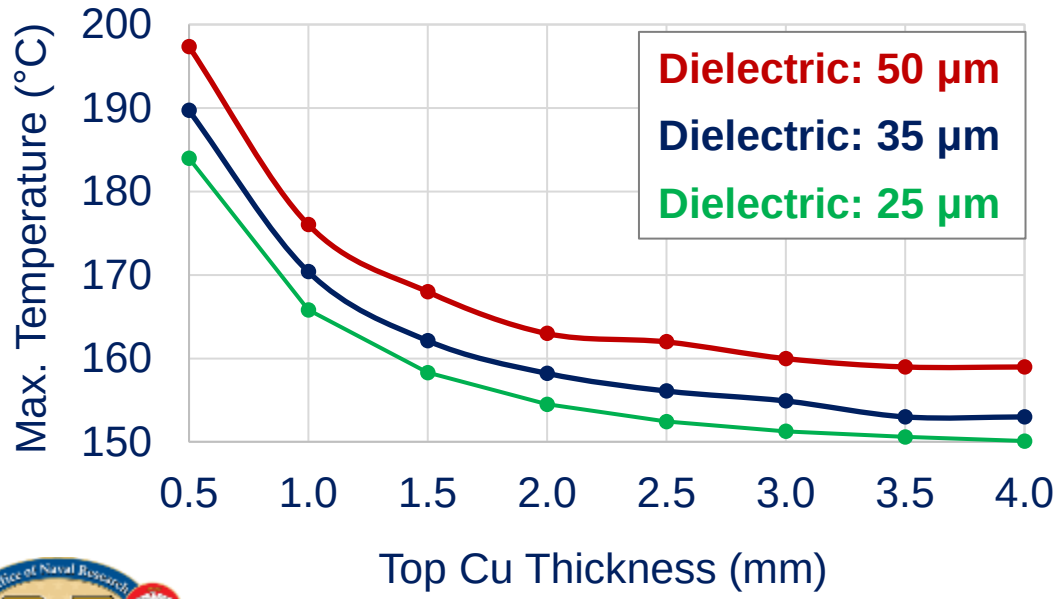
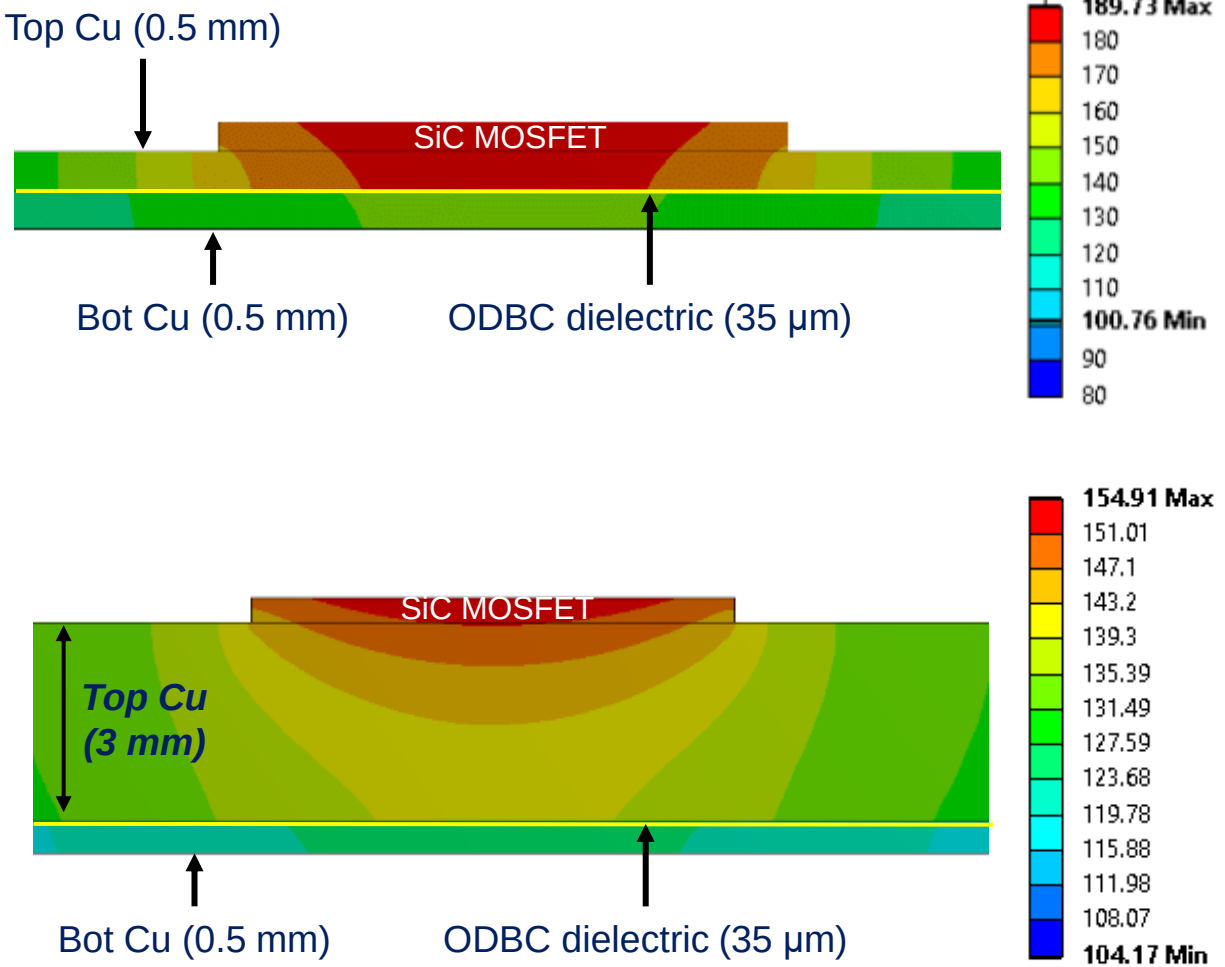
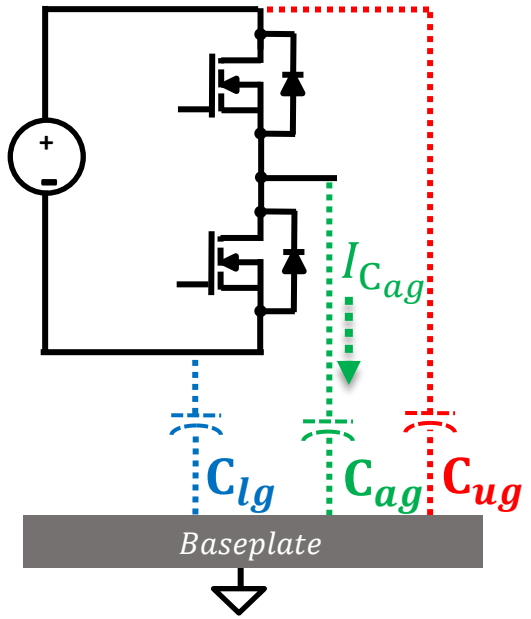


ODBC

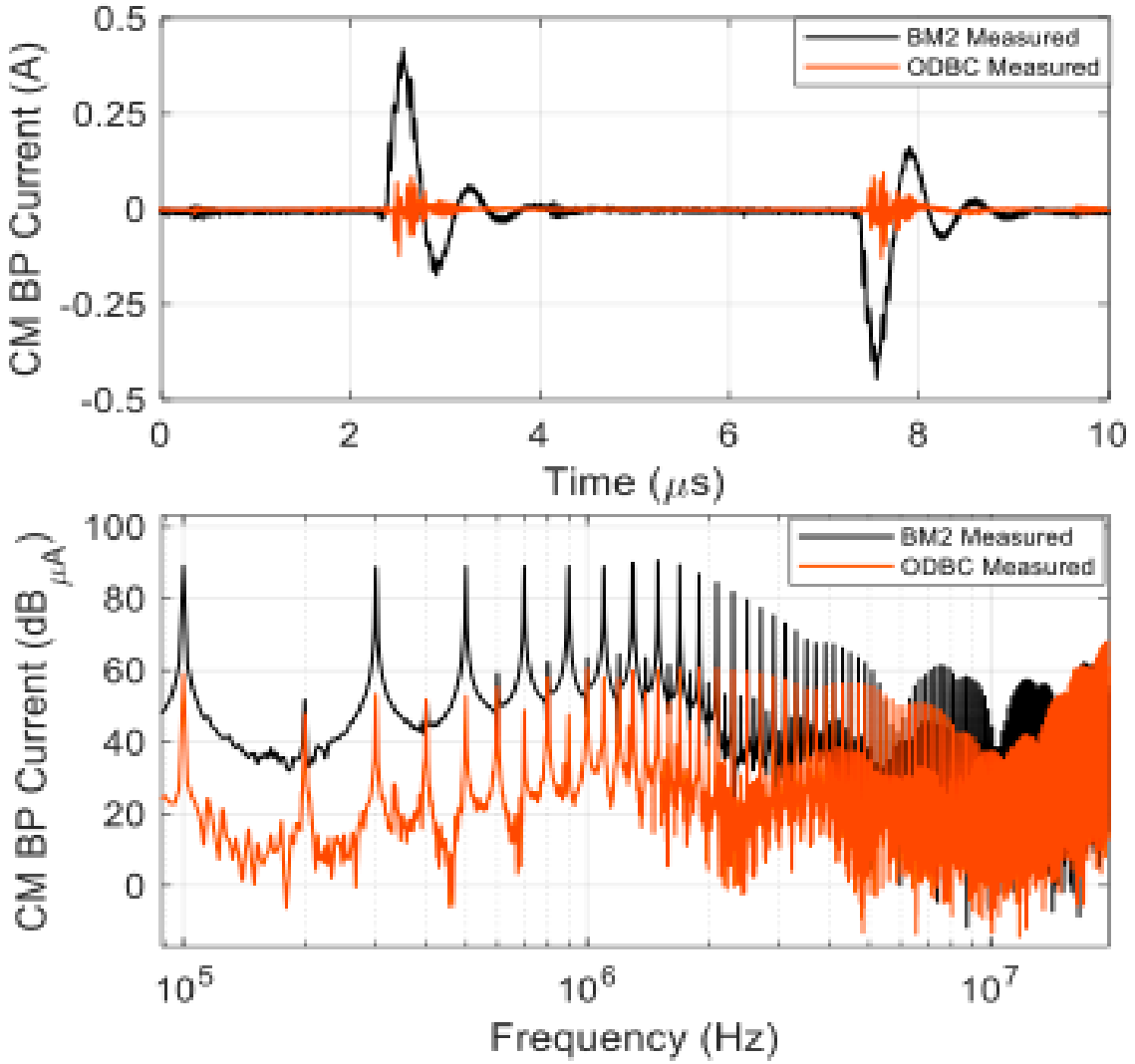


ODBC Challenge: Capacitive Coupling



$$C_{bp} = C_{lg} + C_{ag} + C_{ug}$$

$$q_{ac} = C_{ag} / C_{bp}$$



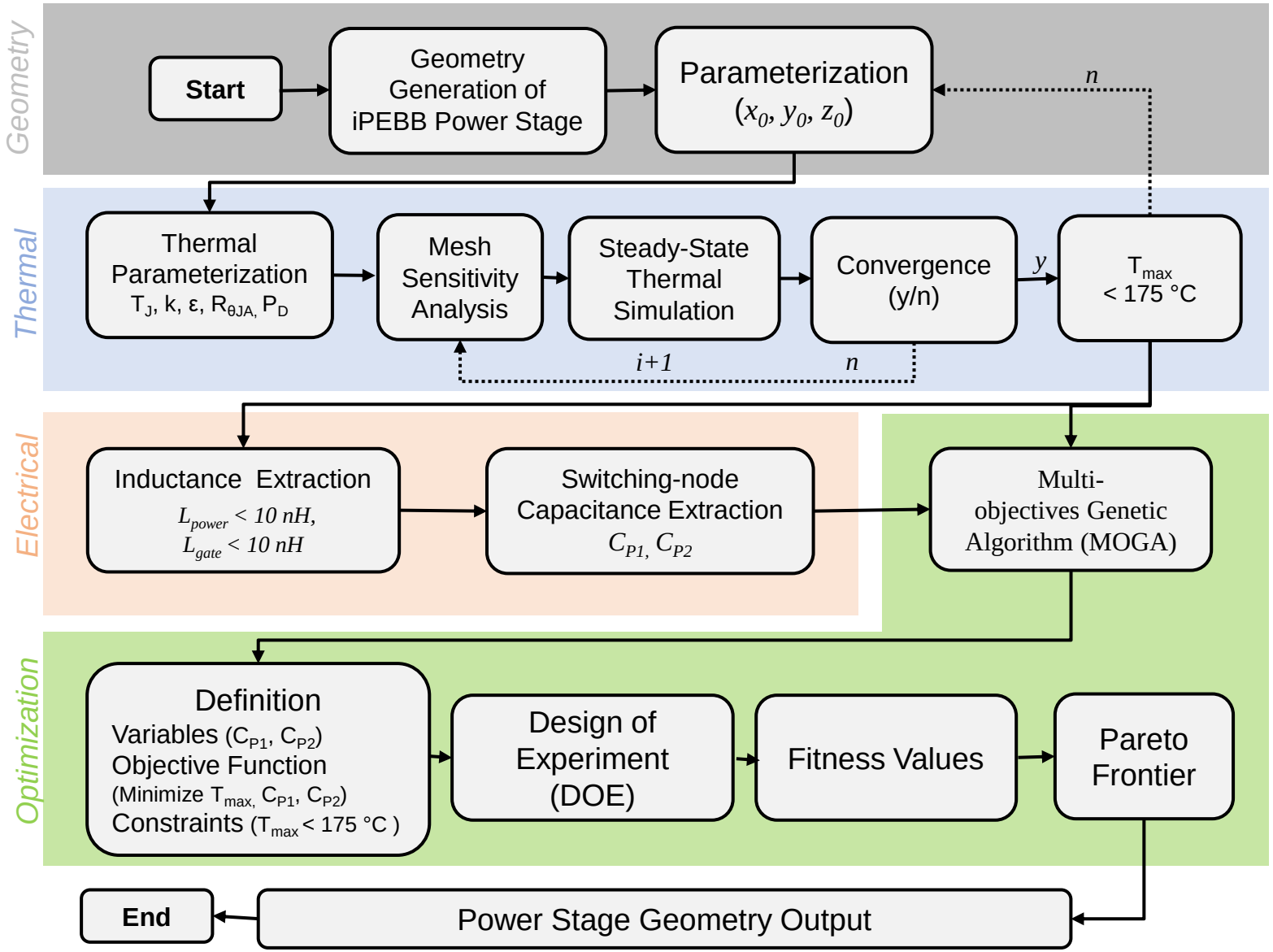
Conventional

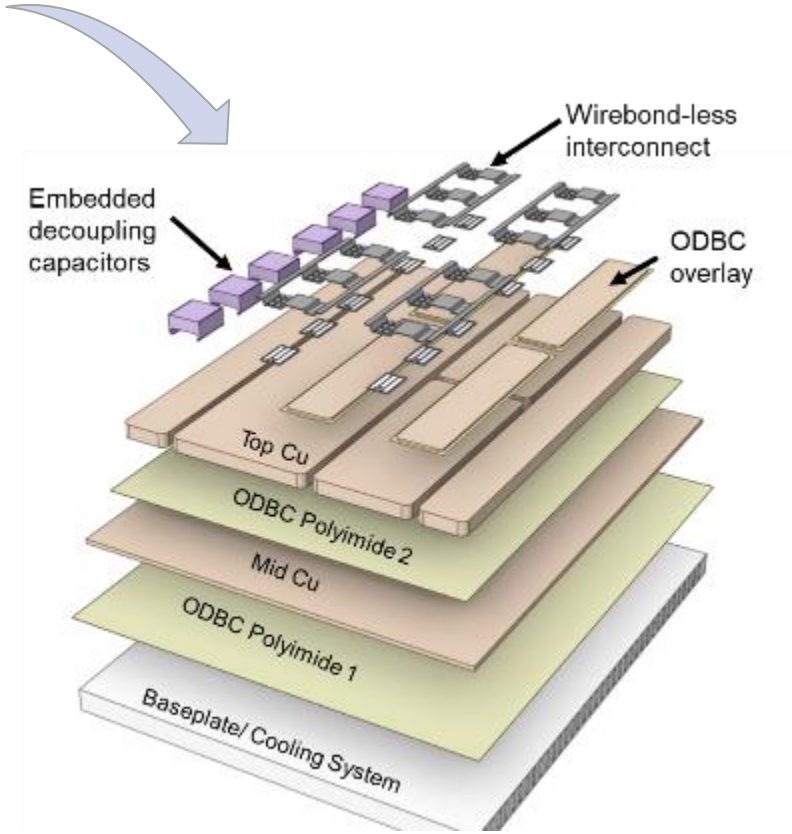
ODBC Module

➢ **35 dB** lower noise through the module baseplate

N. Rajagopal et al., IEEE APEC, 2021, doi: 10.1109/APEC42165.2021.9487439.

Electro-Thermal Modeling Framework





N. Rajagopal et al., IEEE ECCE, 2022, doi: 10.1109/ECCE50734.2022.9947771.

10-kV SiC Module with Stacked DBA Substrates

Co-designed Busbar and Gate Drivers

- ✓**150 V/ns** switching speed
- ✓**1%** voltage overshoot
- ✓**20 x 17 cm²** footprint
- ✓**Drain current sensor**
- ✓**16 kV** partial discharge

10-kV SiC MOSFET Half-Bridge Module

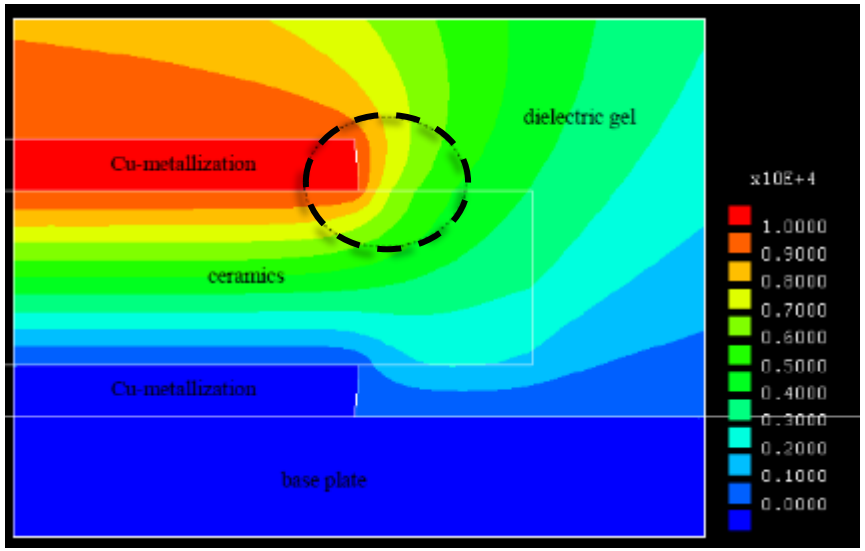
- ✓ **8 x 7 cm²** footprint
- ✓ **5 nH** stray inductance
- ✓ **Wire-bond-less** interconnects
- ✓**>1000 cycles** from –40°C to 200°C

M. Cairnie, C. DiMarino, "Bayesian Optimization of PCB-Integrated Field Grading for a High-Density 10 kV SiC Power Module Interface," in IEEE TPEL, July 2022, doi: 10.1109/TPEL.2021.3128766.
M. Cairnie and C. DiMarino, "Review of Electric Field Reduction Methods for Medium-Voltage Power Modules," CIPS, 2022.

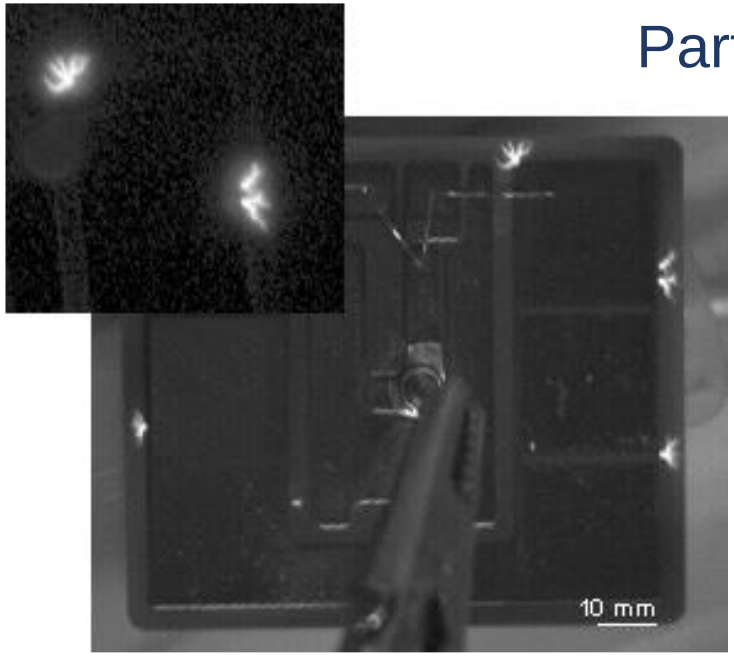
Electric Field Concentration inside Power Modules

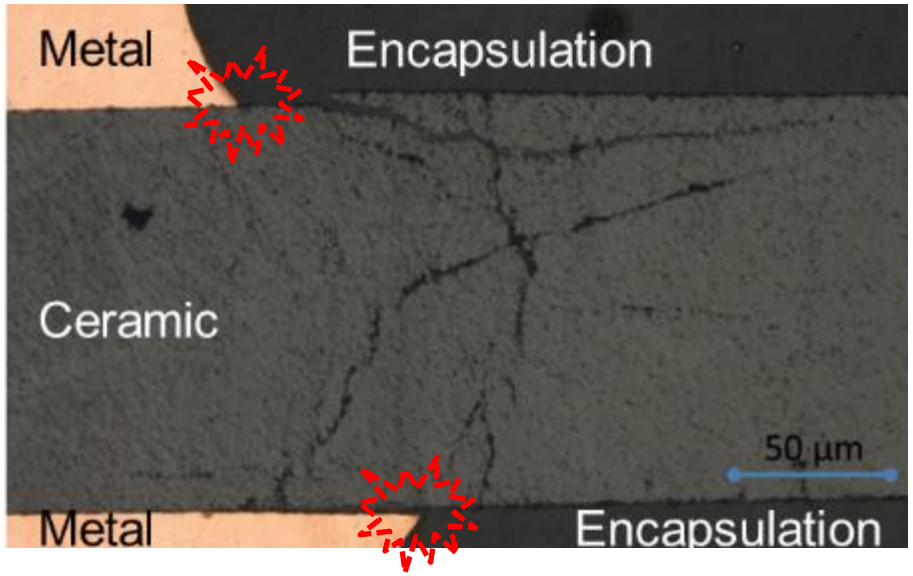
- The electrical field strength is **maximum at the triple point** of the DBC substrate
- The electric field at the triple points does ***not*** follow $\boldsymbol{E = V/d}$

Potential Distribution



Partial Discharge

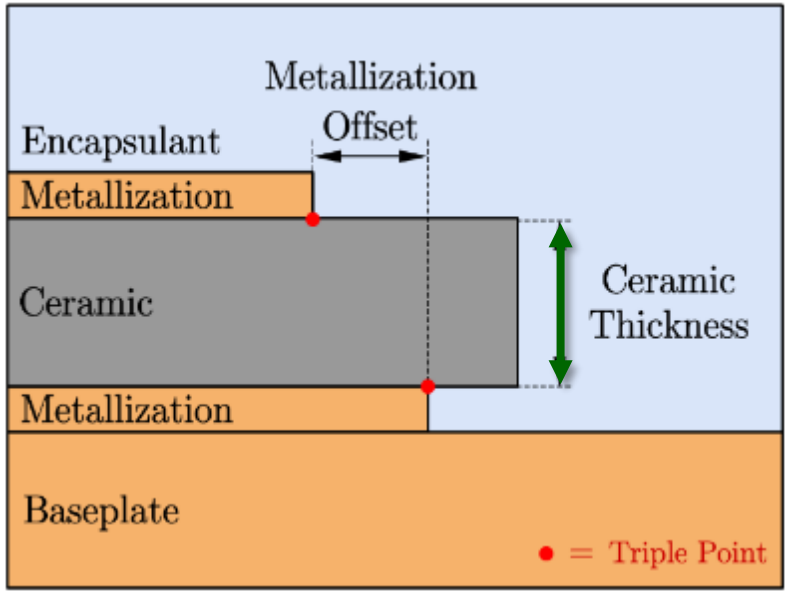




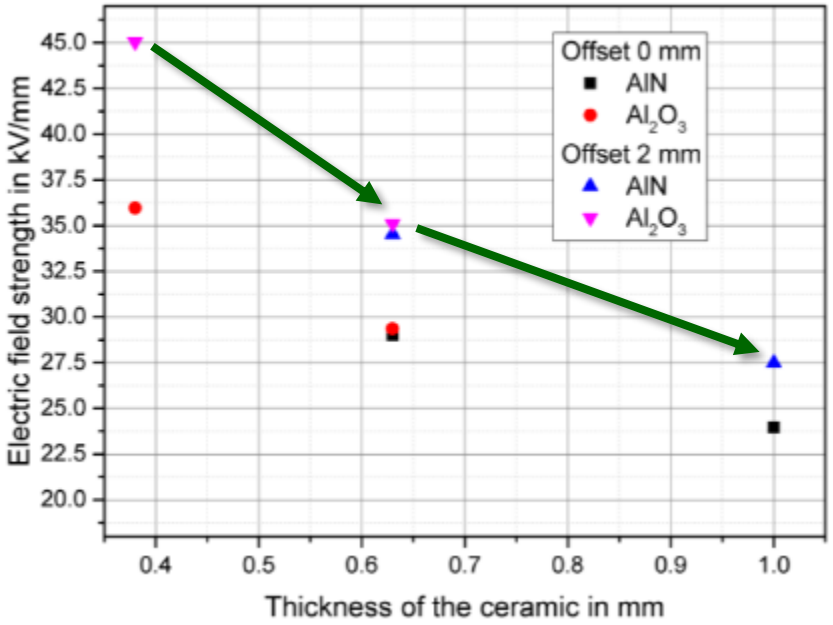
J. H. Fabian, et al., "Analysis of insulation failure modes in high power IGBT modules," IAS Annual Meeting, 2005.
C. Bayer, et al., "Enhancing partial discharge inception voltage of DBCs by geometrical variations based on simulations of the electric field strength," CIPS, 2016.

Ceramic Thickness

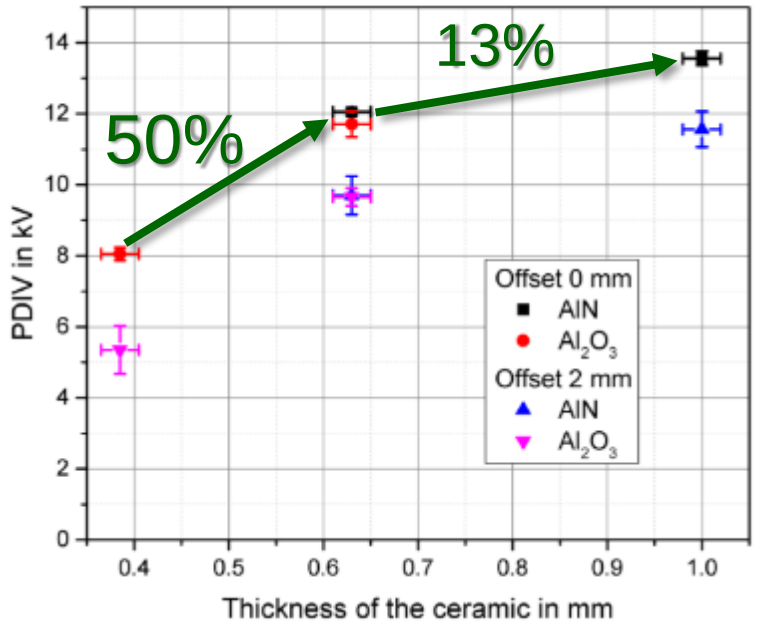
- The electric field at the triple points does ***not*** follow $\boldsymbol{E = V/d}$
- Only **13%** increase in PDIV by moving from 0.63 mm to 1 mm (↑ **59%**)
- $\boldsymbol{R_{th}}$ **increases** with ceramic thickness, so this solution is limited



$\boldsymbol{E}$ Simulations



PD Measurements

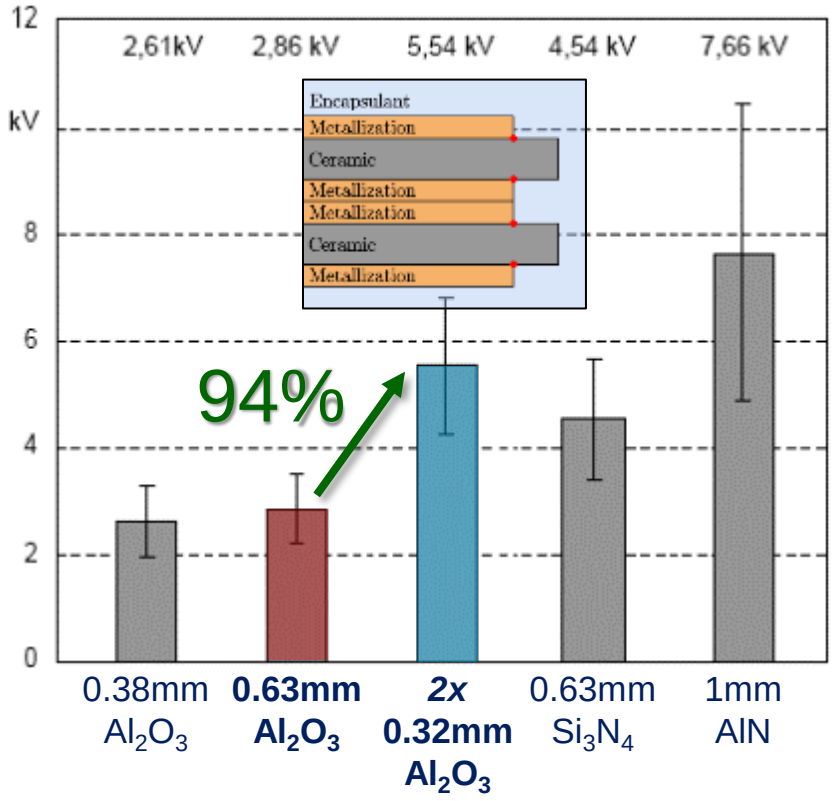


C. Bayer, et al., "Enhancing partial discharge inception voltage of DBCs by geometrical variations based on simulations of the electric field strength," CIPS, 2016.

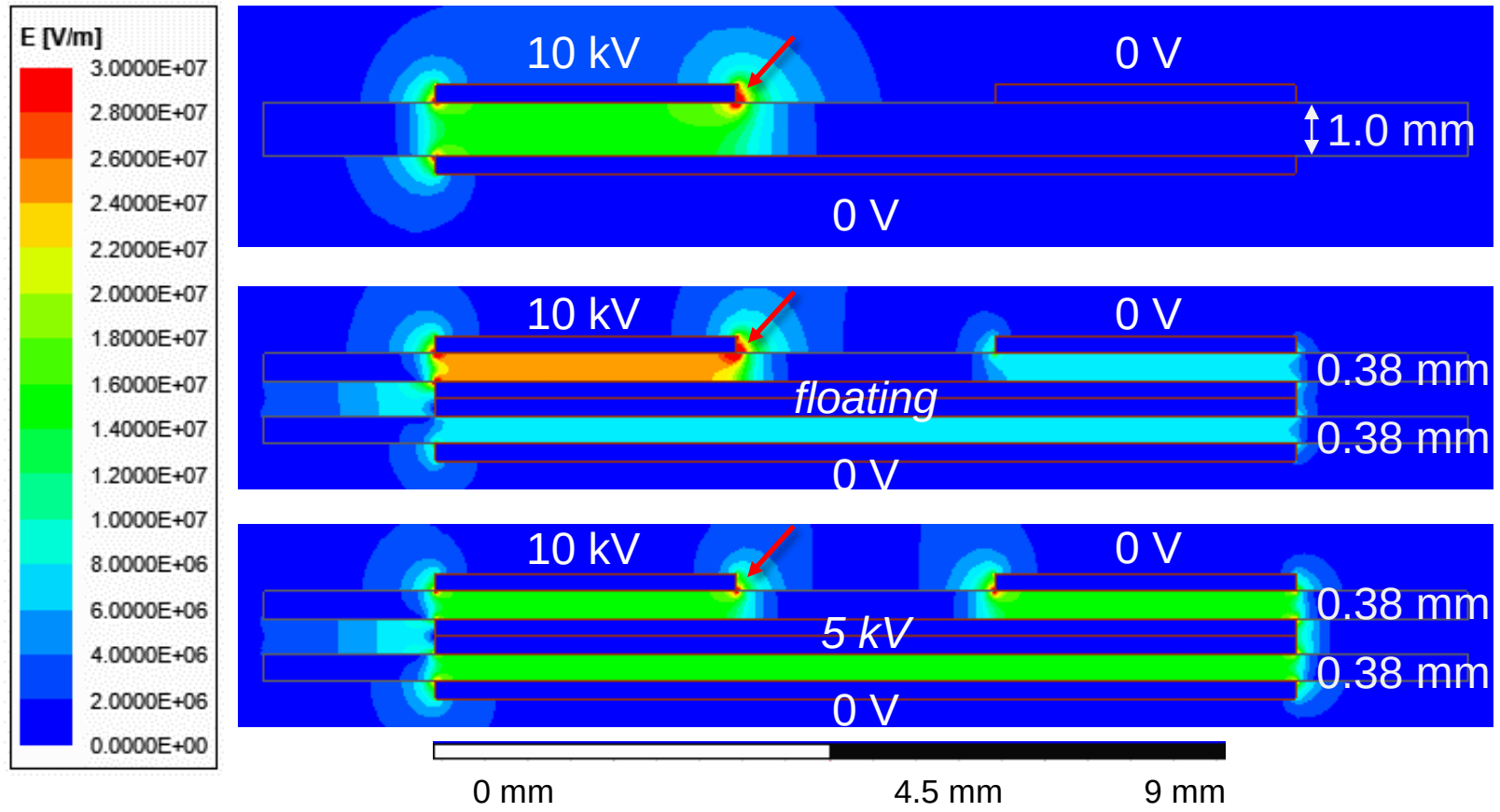
Stacked Substrates

- For **same thickness** (R_{th}), stacking substrates ↑ PDIV by **94%**
- If top layer is patterned, then middle layer should not be left floating

PD Measurements



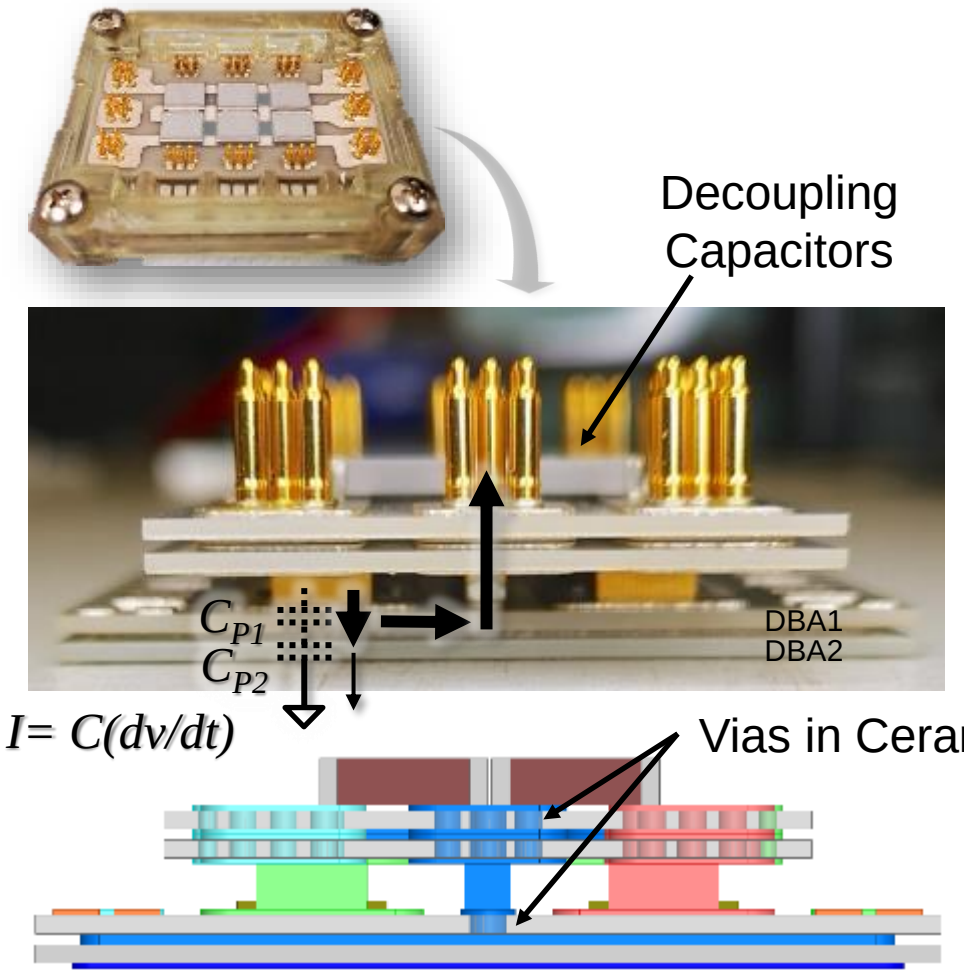
E Simulations

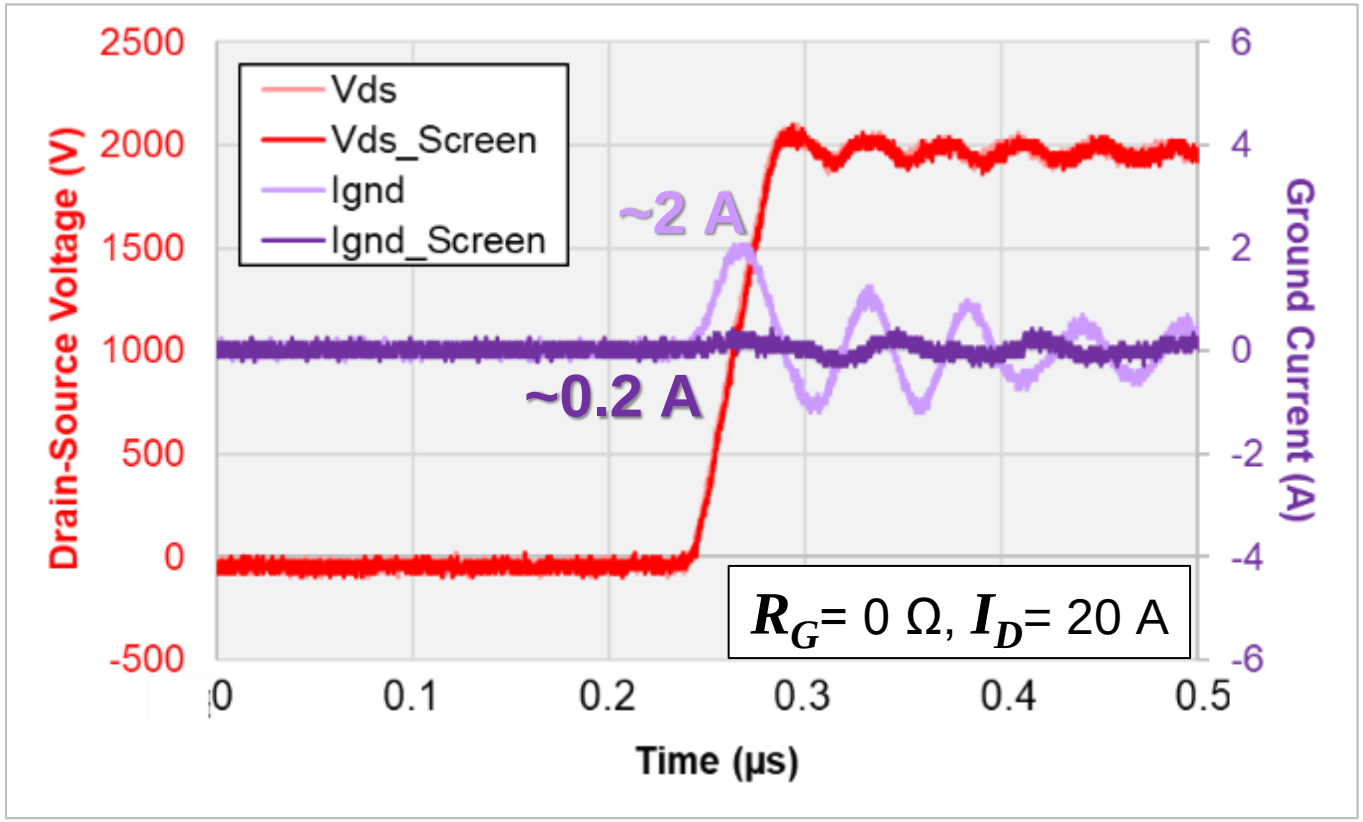


O. Hohlfeld, et al. “Stacked substrates for high voltage applications,” CIPS, 2012.
C. DiMarino et al., IEEE TPEL, 2020, doi: 10.1109/TPEL.2019.2952633.

Stacked Substrates = Integrated Common-Mode Screen

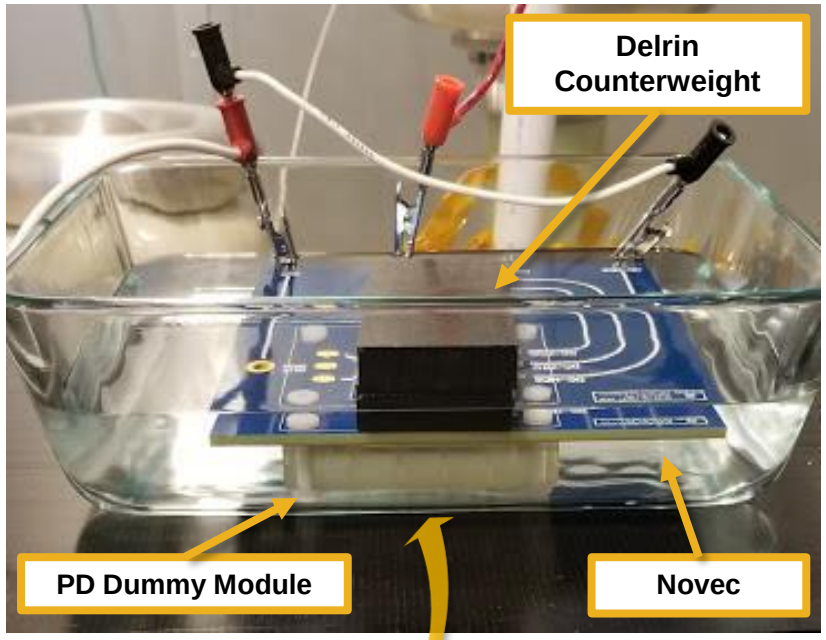
- The middle metal can be used to **reduce the CM current** by **10x**

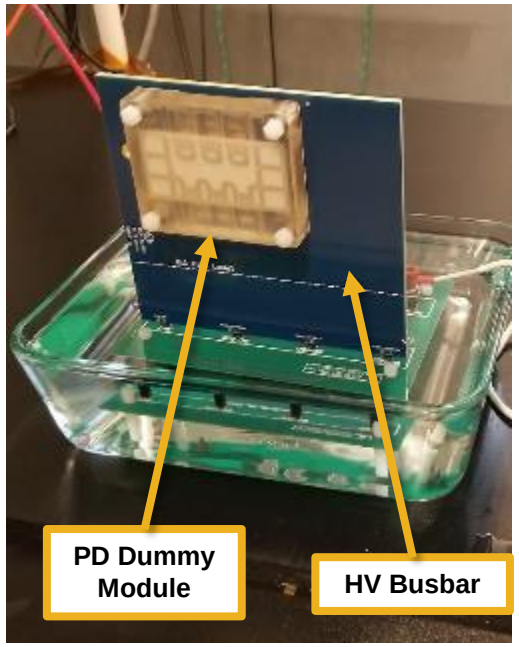


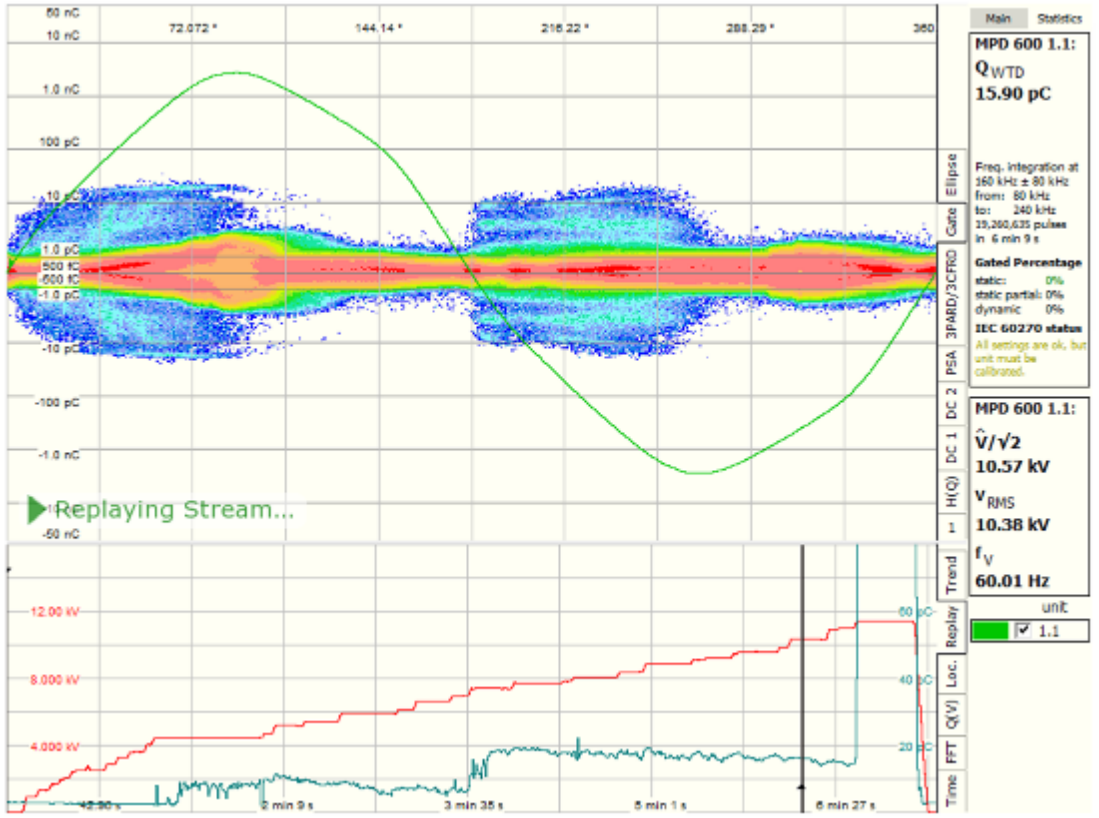


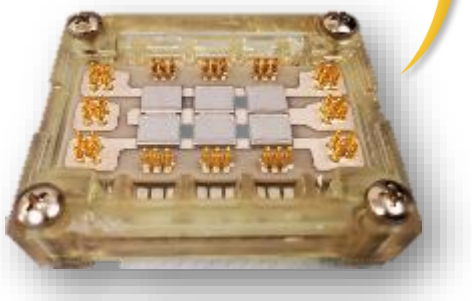
C. DiMarino et al., IEEE TPEL, 2020, doi: 10.1109/TPEL.2019.2952633.
C. DiMarino et al., U.S. Patent 10032732, 2018.

Partial Discharge Measurements









- **16.4 kV** partial discharge inception voltage

M. Cairnie, C. DiMarino, IEEE TPEL, 2022, doi: 10.1109/TPEL.2021.3128766.
M. Cairnie and C. DiMarino, "Review of Electric Field Reduction Methods for Medium-Voltage Power Modules," CIPS, 2022.

Conclusions

- Heat dissipation, EMI, and insulation are limitations to full utilization of WBG and UWBG devices
- PCB-embedding is a promising technology for high integration and enables good thermal performance and efficiency
  - Limited current/power
- Organic / IMS substrates offer larger footprints, dissimilar metals, thicker metals, and multi-layer structures
  - Low thermal conductivity and high capacitive coupling
- Stacked / multi-layer ceramic substrates can be used for reducing E field and common-mode screening
  - High cost
- New architectures, cooling, design tools, materials, and methodologies are needed to overcome present limitations

Thank you!

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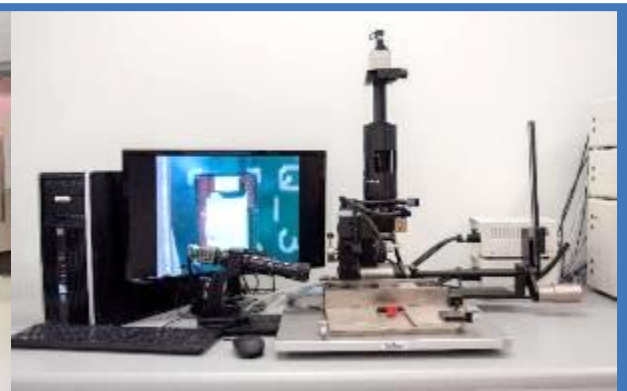

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