Heterogeneous Integration Roadmap

Integrated Power Electronics (IPE)

Technical Working Group: Chapter 10

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Integrated Power Electronics (IPE) Technical Working Group (TWG)

3D-PEIM International Symposium on 3D Power Electronics Integration and Manufacturing

HIR Heterogeneous Integration Roadmap

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Today is Groundhog Day

- Punxsutawney Phil saw his shadow and predicted 6 more weeks of winter
- Groundhog predictions have had a 39 % success rate
- Random guess has a 50% success rate
- We hope our Roadmap Predictions are better than the groundhog!

Heterogeneous Integration of Power

The integration of separately manufactured power electronic components and subsystems into higher-level assemblies that provide enhanced functionality and improved operating characteristics.

Critical to: ***efficiently*** ***distribute*** ***clean*** ***power to*** ***multiple*** ***IPs*** ***requiring*** ***different*** ***voltages*** ***and*** ***currents***

- **Efficiently** - Reduce power loss so as to minimize need for cooling
  - Wide bandgap power devices that can operate at high frequency (e.g. GaN)
  - New trace/via materials and shorter lengths to reduce interconnect/winding resistance
  - Zero voltage, low capacitance, switching to reduce loss; lower core loss inductors
  - Thermal isolation through glass and low k substrates, thermal metamaterials on layers
- **Clean** – Minimize noise generated in the devices by power distribution
  - Shielding, filtering, low permeability materials, reduced coupling, eddy currents – low EMI
  - Lower inductance through flip chip, Cu bumps, HDI, SiPLIT to lower ΔI noise
  - Decreased power path impedance
  - Decoupling – put power transmission on every interconnect level.
- **Multiple** – Distribution to many different devices and device types
  - Efficient scheme to minimize conversions to reduce losses
  - Reduced size embeddable converters close to the devices being powered
  - Multiphysics simulation, co-design and leverage AI

Heterogeneous Integration of Power Roadmap

3D-PEIM International Symposium on 3D Power Electronics Integration and Manufacturing

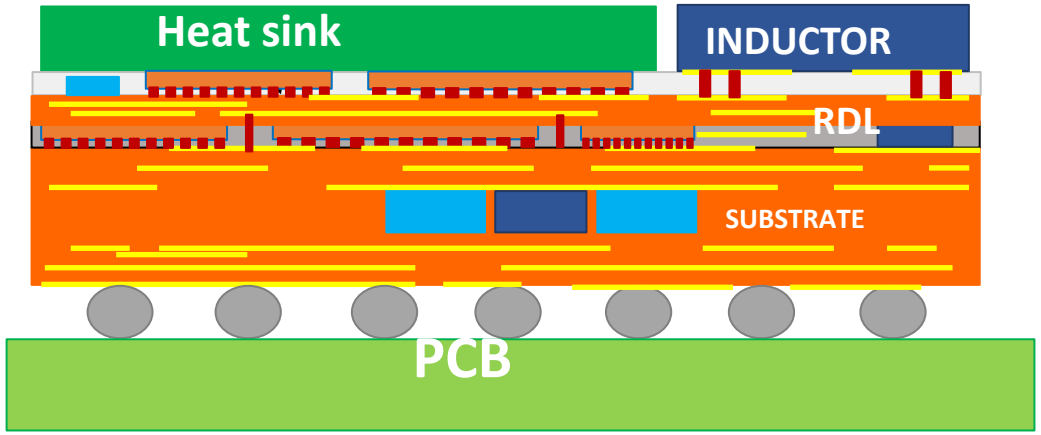
HIR Heterogeneous Integration Roadmap

Latest update to HIR Chapter 10

- Section 1
- Section 2
- Section 3
- Section 4

Integrated Power Electronics Components for

- Integrated voltage regulators *(IVRs)* Up to 5V
- Power System in Package Modules 5-100V
- Integrated High Power Systems >100V
- Energy Harvesting



Agenda for each section:

- Challenges
- Metrics
- Potential solutions
- Required R&D

IEEE PELS ITRW Roadmap

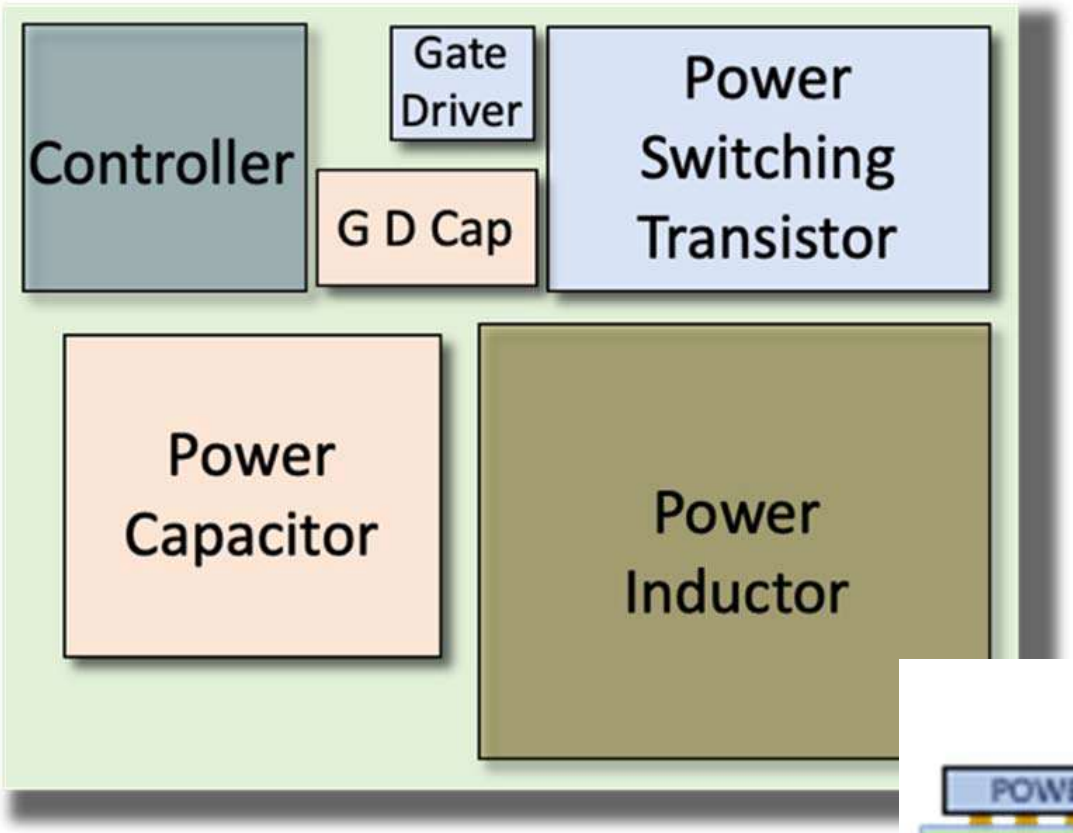
Cooperation

IEEE EPS HI Roadmap

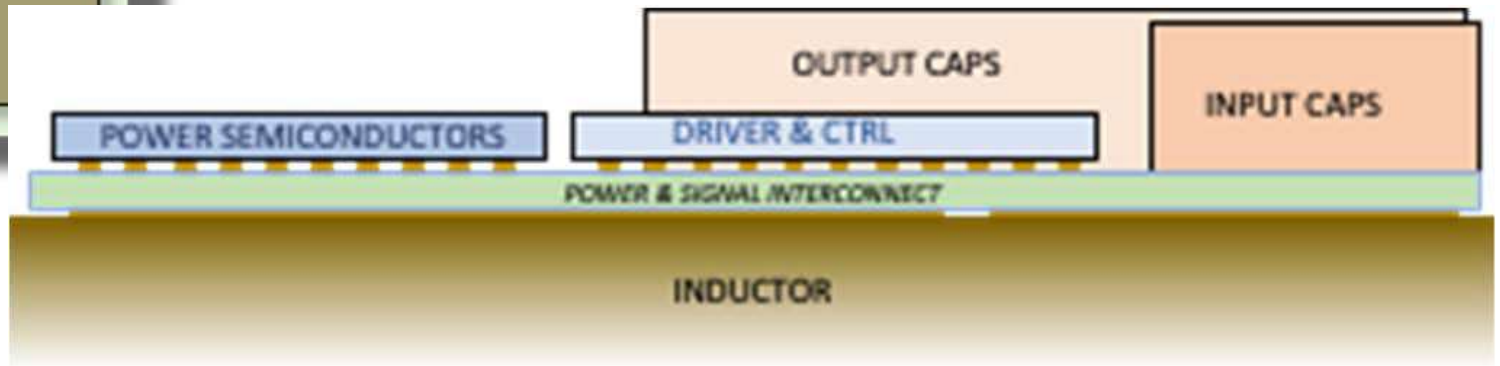
IEEE | IEEE photonics Society | semi | IEEE Electronics Packaging Society | ASME

Electron Devices Society

What is an Integrated Power Electronic Component (IPEC)

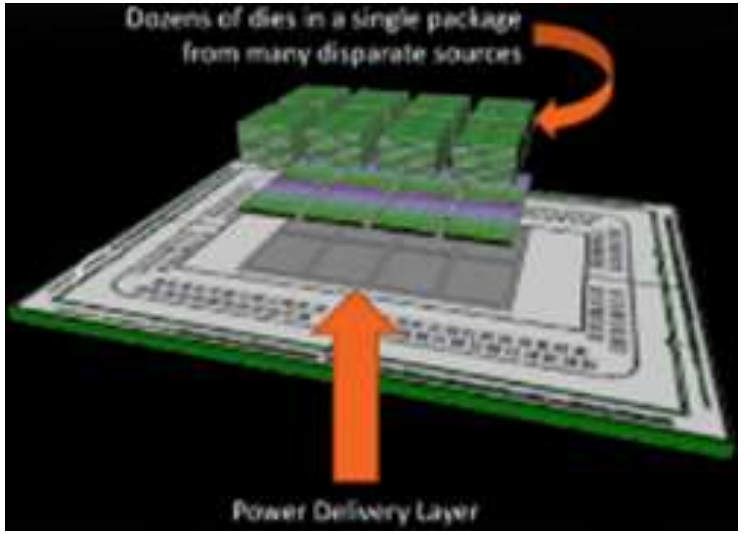


The "Integrated Power Electronics Component," IPEC, represents the electrical components and functions required for electronic conditioning of electrical energy delivered to the load(s).

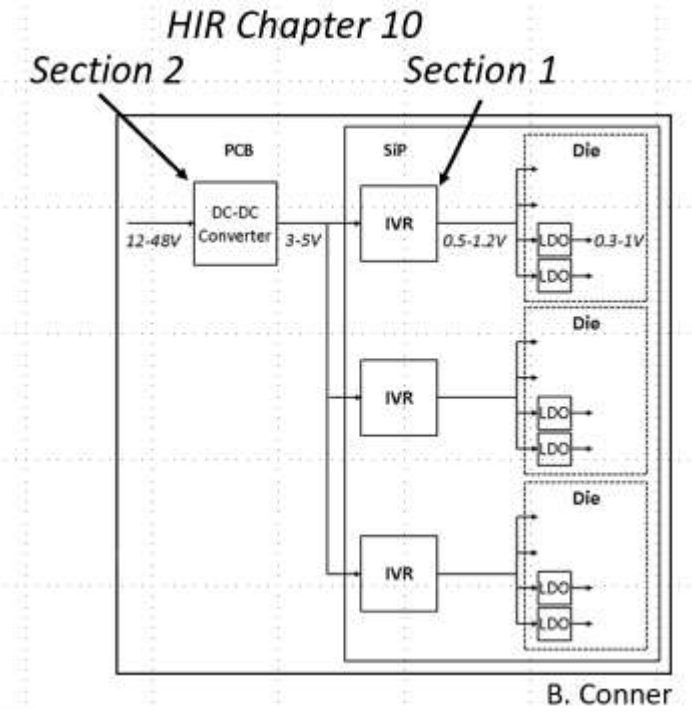


IPECs for Integrated Voltage Regulators (IVRs)

- Fine-grain power management significantly improves energy efficiency (performance-per-watt) by up to 73% by supplying the minimal voltage required at any given time to each load.
- It requires Integrated Voltage Regulators (IVRs) located in close proximity to the load to bypass the majority of the power distribution network (PDN) and associated impedance.
- PCB mounted voltage regulators (VRs) cannot supply accurate voltages due to their high PDN impedance.
- The way forward is PCB-mounted DC-DC converters that step down system bus voltage to an intermediate voltage, which is input to IVRs.

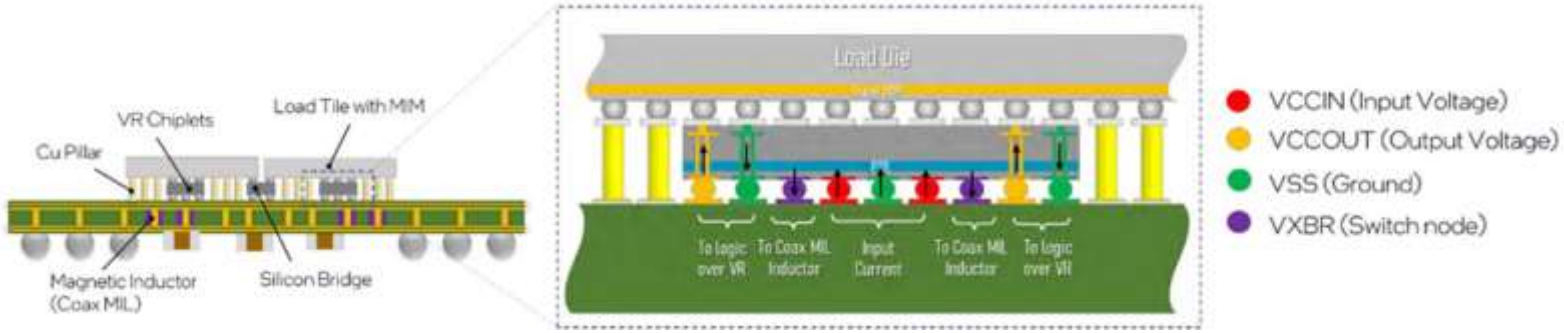


IVRs Integrated in SiP in Close Proximity to Loads



Approaches to Heterogeneous Integration for IVR

- Disaggregate and tightly re-integrate separately manufactured components in a high reliability, low cost IPEC that provides multiple precisely regulated voltage outputs:
  - Over a wide range of voltage (0.5 – 1.8V)
  - With increasing input voltage (3-5V)
  - At current density (10-20A/mm)
  - And switching frequency (5-50MHz)
  - With an ultrathin z-dimension (100µm or less).
- Integrate IPECs in SiPs under the load die similar to silicon bridges, to provide vertical current flow for each voltage rail to its load from the PCB through the package substrate to the load die
  - Minimizes lateral current flow and associated parasitics
  - Significantly improves PDN and fine-grain power management.
  - Capacitors may be integrated in the load die and/or the IPEC.
  - Inductors may be integrated in the IPEC or package substrate



Metrics: IPECs for IVRs

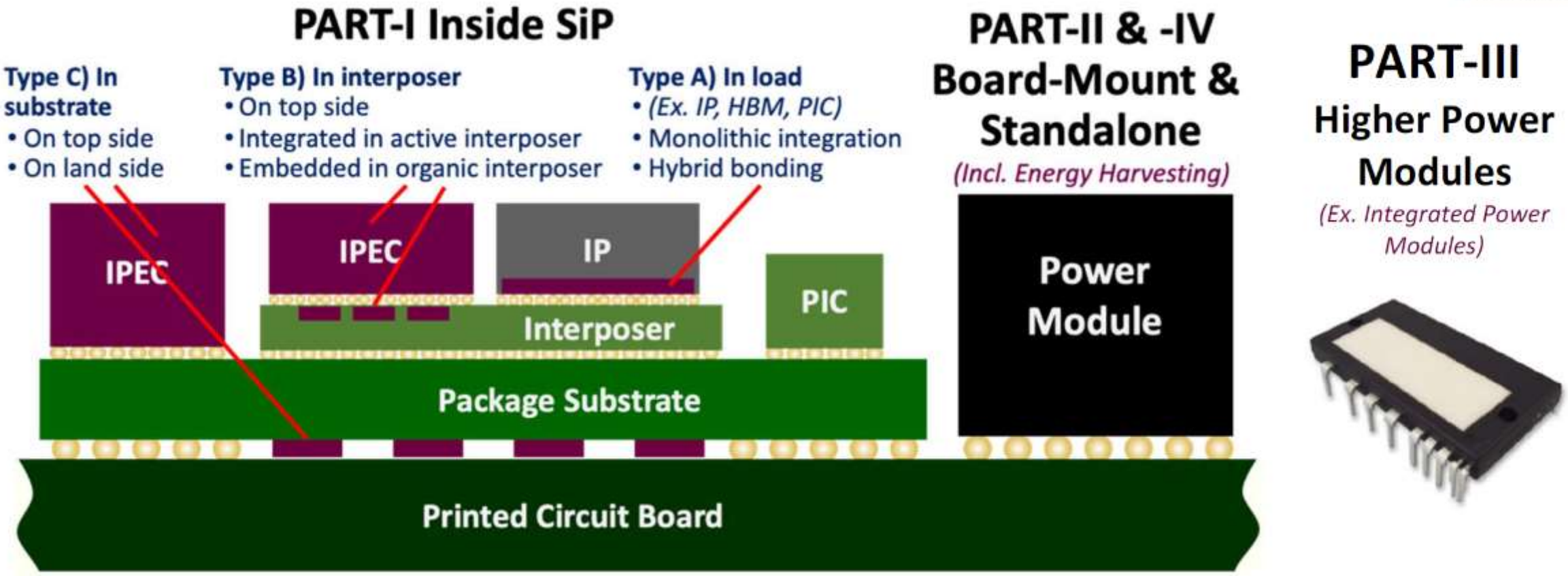
Metric	Generation			
	1	2	3	4
Input voltage (V)	3	3	5	5
Switching Frequency (MHz)	5 - 10	10 – 50	5 - 10	10 - 50
Output current density (A/mm²)	10	20	10	20
Output voltage (V)	0.5 - 1.2			
Thickness (μm)	100			

Reduce routing loss
Shrink passives, increase transient response
Support many rails / phases
Minimize power loss
Ultra-thin for embedding in SiP

Plus:

- **High efficiency**
- **Ultra-low thermal resistance**
- **High reliability**
- **Low cost**
  - **Made with panel- vs. wafer-level processes**
  - **High yield**
  - **Known good die**
  - **Modularity**

How Are IPECs Integrated into SiPs?

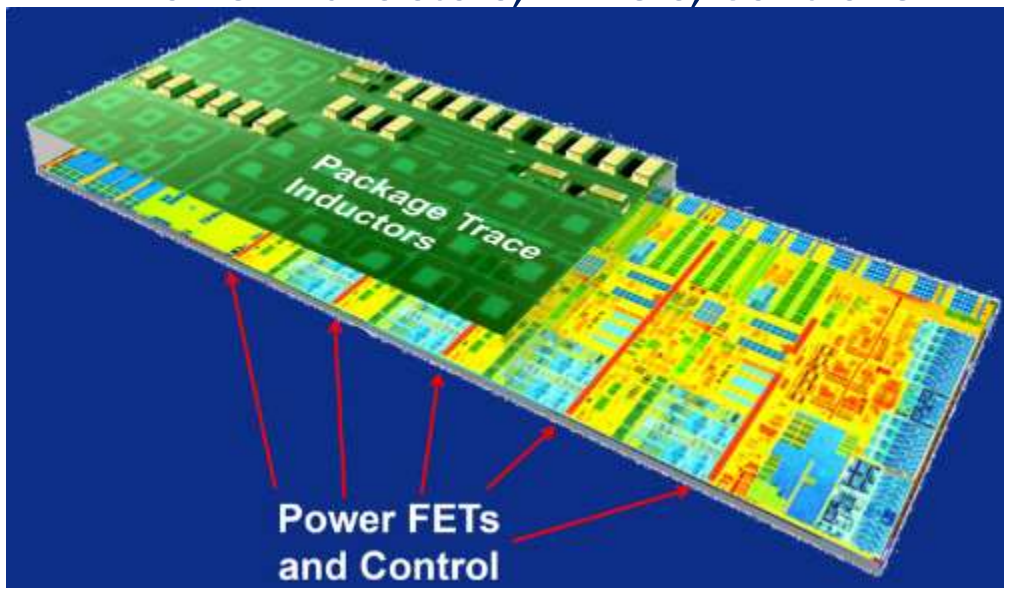


IPECs may be partitioned and integrated in multiple ways, each potentially serving different parts of hybrid topologies

IPEC Type A: Integrated in Load

Monolithic Integration

Power Transistors, Drivers, Controller

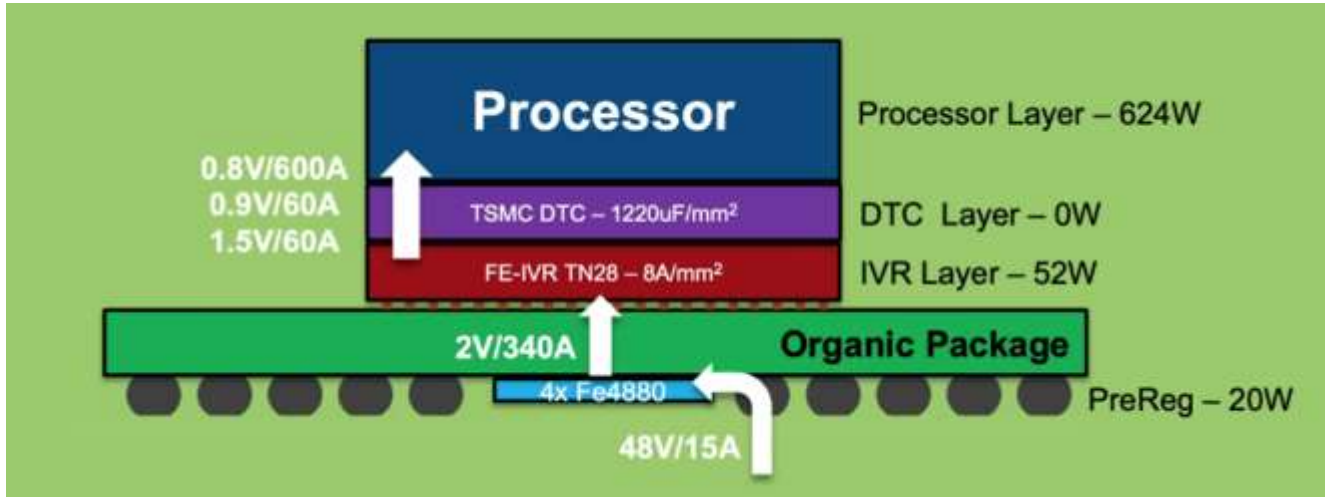


Package and Platform View of Intel's Full Integrated Voltage Regulators (FIVR)

Hybrid Bonding

Integrate a hybrid converter topology:

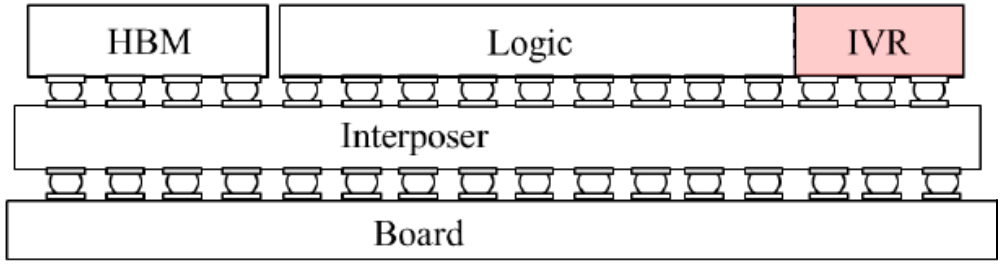
- 1st stage: 48V-to-2V converter on landside of package
- 2nd stage: hybrid-bond deep trench capacitor (DTC) and integrated voltage regulator (IVR) layers to the processor dies



IEEE Power Electronics Society October 22, 2020, Integrated Power – A Virtual Panel Session

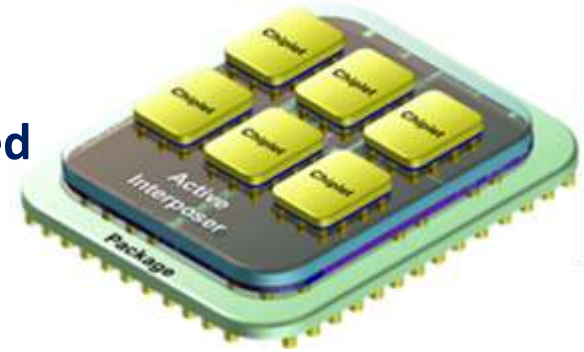
IPEC Type B: Integrated in Interposer

On Top



Power Integrity Comparison of Off-chip, On-interposer, On-chip Voltage Regulators in 2.5D/3D ICs

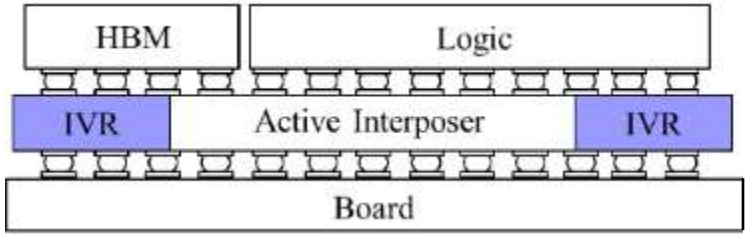
Monolithically Integrated in Active Interposer



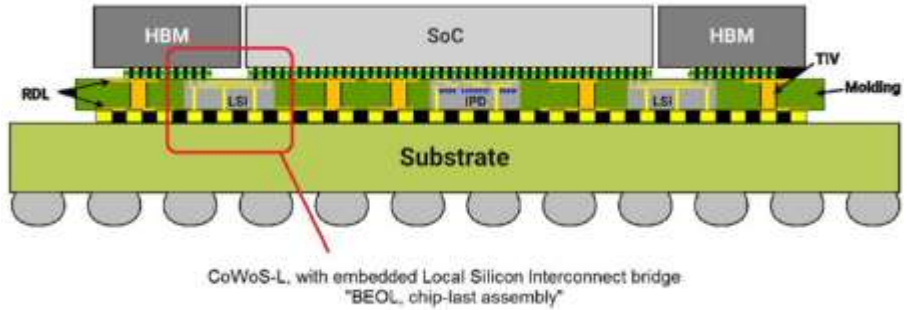
From "CEA-Leti to Collaborate with Intel on 3D Packaging Technologies"

A 220GOPS 96 Core Processor with 6 Chiplets 3D Stacked on an Active Interposer offers 0.6ns/mm Latency, 3Tb/s/mm^2 Inter-Chiplet Interconnects, and 156mW/mm^2@ 82%-Peak-Efficiency DC-DC Converters

Embedded in Organic Interpower



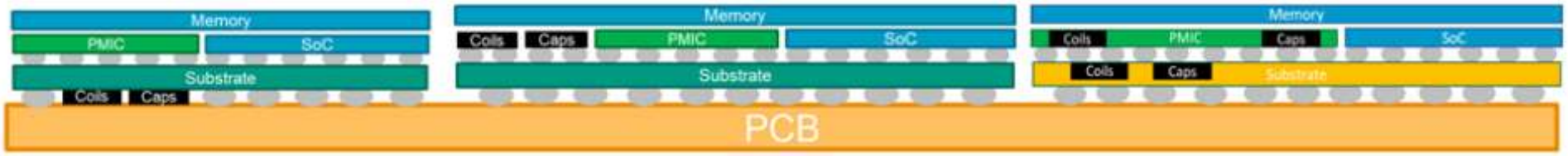
Power Integrity Comparison of Off-chip, On-interposer, On-chip Voltage Regulators in 2.5D/3D ICs



TSMC Co-Wo-S-L

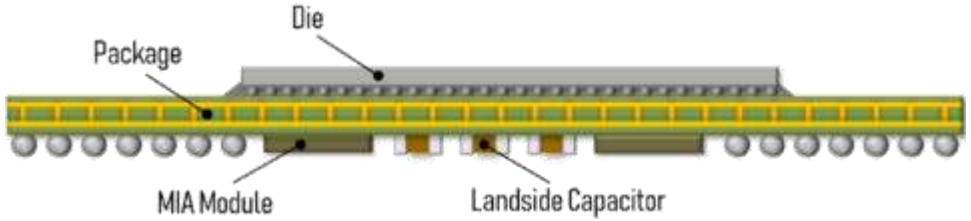
IPEC Type C: Integrated in Substrate

On Top



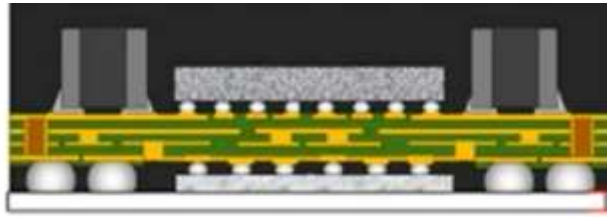
Voltage Regulators with Integrated Inductors on Chip vs in Package

On Bottom

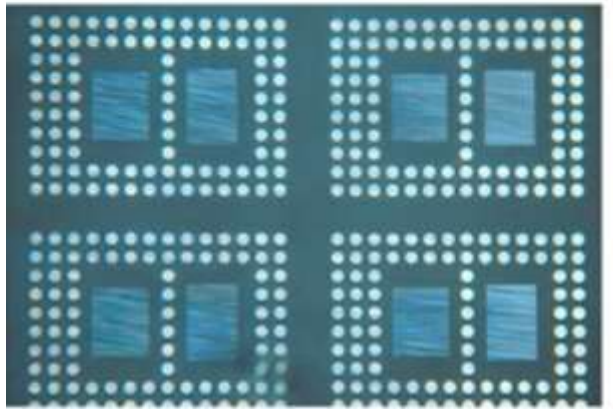


Magnetic Inductor Arrays for Intel® Fully Integrated Voltage Regulator (FIVR) on 10th generation Intel® Core™ SoCs

- Monolithically integrate on processor die 1.8V MOSFETs, drivers and controllers for many buck regulators
- Magnetic inductor array (MIA) and capacitors on landside of package
- External PCB-mounted voltage regulators still required to supply 1.8V



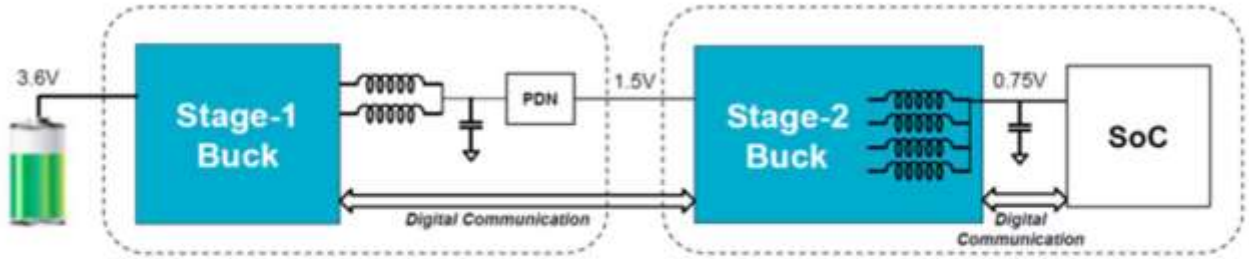
ASE's Double-Sided Mounting SiP



2020 11 18 IMAPS' webinar
Enabling a Path to System Level Solutions

Stand-alone SiP

Stand-alone on-board power SIP modules also play an important role in delivering power to most of the system components. They consist of switches, drivers and controllers, along with the storage elements such as passives. Use multi-level power conversion



Key Parameters include:

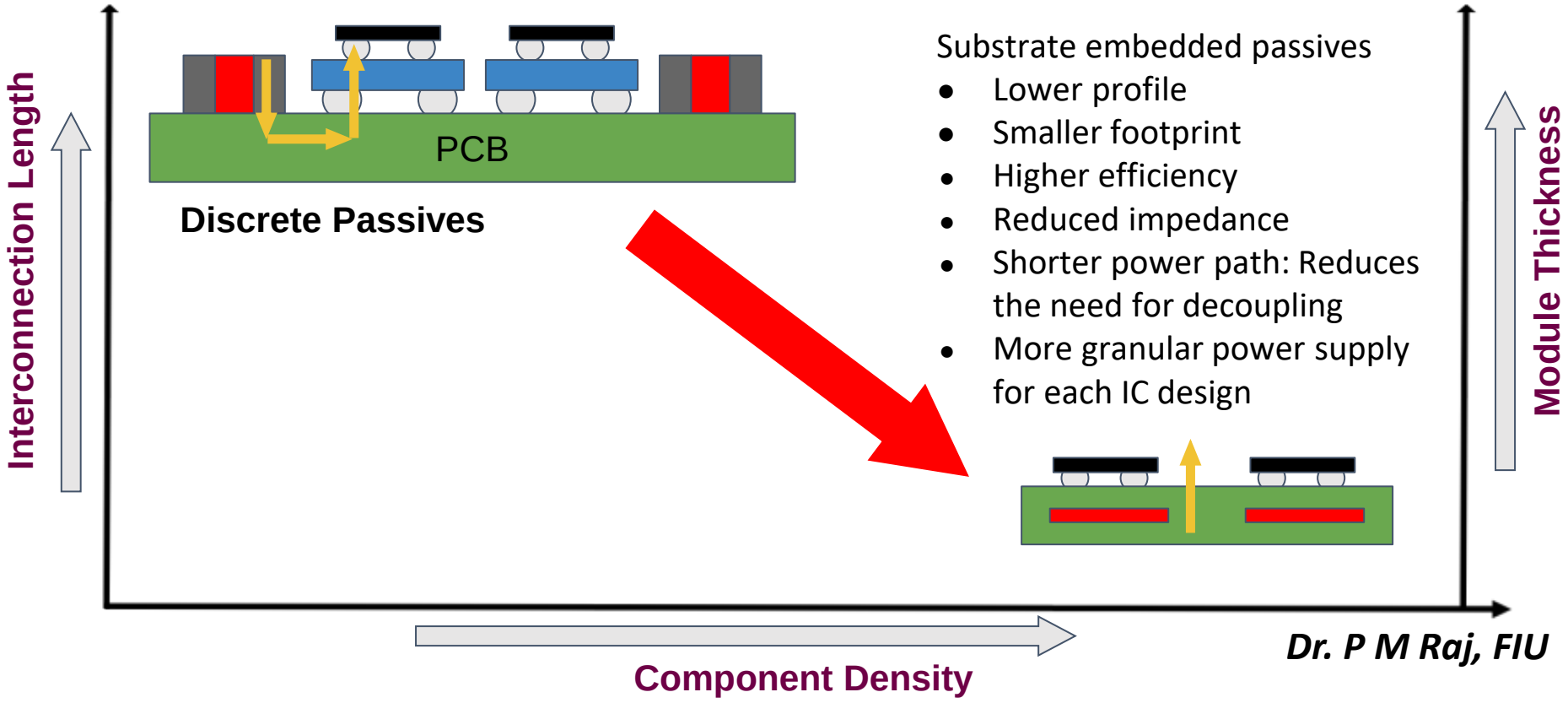
Application	Vin	Vout	I	Efficiency	di/dt	DVFS	Ripple
Server processor	12-48 V	~1 V	~100 A	High at high current	High	Low	Medium
Graphic processor	12-48 V	~1 V	100's A	High at high current	Low	Low	Medium
AI accelerator	12-48 V	~1 V	100's A	High at high current	Low	Low	Medium
Mobile processor	2.3-5 V	~0.4-0.8 V	~5 A	High 10 mA to 3A	High	High	Medium
HBM Module	3.3-5-12 V	~1 V	~10 A	High at high current	Low	Low	Medium
Optical module	3.3 V	~0.4-0.8 V	~10 A	High at high current	Low	Low	Small
Cell Baseband processor	5-12 V	~1 V	~5-20 A	High at high current	Low	Low	Small

SiP Power Module Advancements Needed

- Increased volumetric density of passives without sacrificing efficiency & power handling.
- High Tg (>250°C) substrates with low moisture absorption, resistance to electrochemical migration at high temperature and humidity.
- Devices with copper termination
- Backside metallization of dies compatible with direct bonding on copper leadframes or packages.
- Pressureless assembly of dies with nanosilver and nanocopper.

Metric	2022	2025	2028
Power Density (3-5V)	200 W/in³	500 W/in³	1000 W/in³
Current Density	0.1 A/mm²	0.4 A/mm²	2 A/mm²
Frequency	1-5 MHz	10-20 MHz	50-100 MHz
Voltage (Processor)	0.8 V	0.6 V	0.6V
Module Thickness(3-5V)	0.8 mm	0.6 mm	0.4 mm
Peak Efficiency (3-5 V)	86%	88%	88%
Peak Efficiency (48 V)	50 W/in³	100 W/in³	300 W/in³
Power Density (48 V)	95%	95%	95%

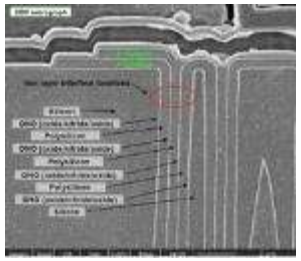
Need for Embedded Power Passives



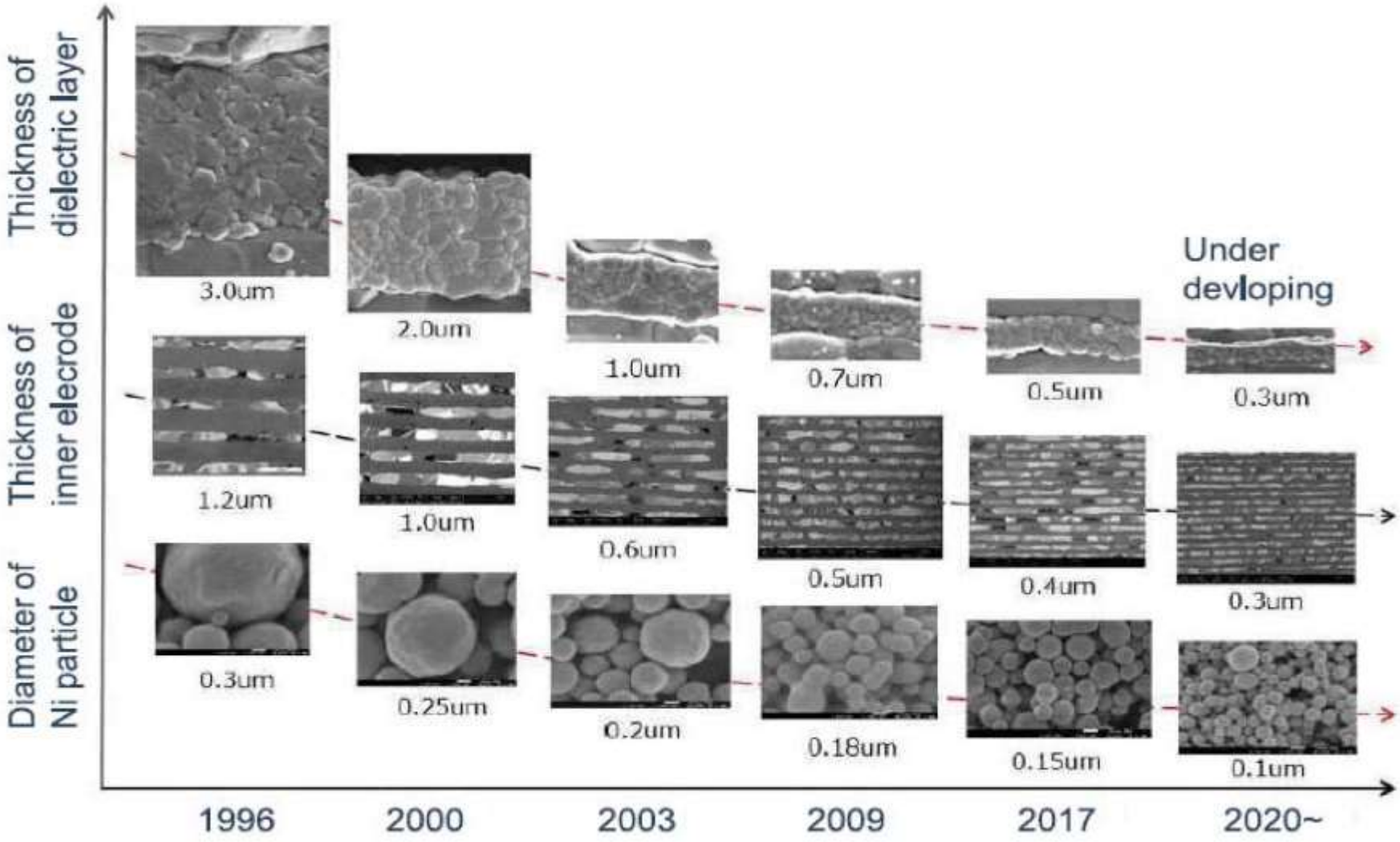
Capacitor Technologies

Dr. P M Raj, FIU

	Thin MLCC	Trench Caps	Ta Chip	Emerging Need
Volumetric Density	20 µF/mm^3	10 µF/mm^3	~10 µF/mm^3	50-100 µF/mm^3
Thickness	100 µm	100 µm	600 µm	50-100 µm
Freq. Stability	10-100 MHz	>1-10 MHz	0.2 -1 MHz	>10 MHz
ESR	~10 mΩ	50 mΩ x µF	>100 mΩ x µF	~50 mΩ x µF
% ΔC/V	-13 % to -70% (1 to 4 V)	~ 0 %	~ 0 %	~ 0 %
Max. Temp	85° C	150° C	125° C	>125° C
	PICK AND PLACE			FILM EMBEDDING WAFER OR PANEL INTERCONNECTS



MLCC Evolution [Murata]



Embedded Capacitors Roadmap

Board or package embedding; I/O decoupling; 100 MHz

Embedded polymer laminate and dielectrics

- 0.1 nF/mm² Polymer laminate dielectrics
- 0.5 nF/mm² Polymer film dielectrics
- 1 nF/mm²

Embedded ceramic film

- 2-3 nF/mm² Thin oxides
- 20-30 nF/mm² BaTiO3 film
- 30-50 nF/mm² enabled by new multicomponent oxides

Package embedding; Core and I/O decoupling; 100-500 MHz

Capacitors – wafer

- Silicon capacitors Deep trench 0.08 µF/mm² 0.25 µF/mm² 0.5 µF/mm²
- Ultra-high surface area Si 1-2 µF/mm²
- Multilayered dielectrics on deep trench

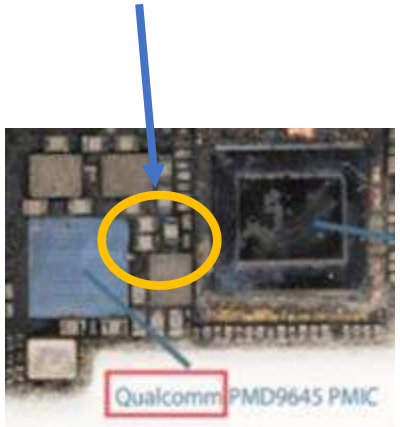
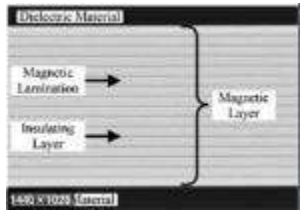
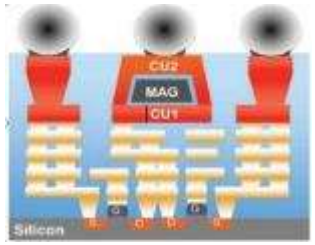
IVR; Embedded PoL 1-20 MHz

Formed capacitors – panel

- Adv. Nanotech. >3 µF/mm²

Dr. P M Raj, FIU

Inductor Technologies

	Discrete (Ferrite or Metal Powder)	Magnetic composites – substrate-embedding	Nanomagnetic films: On-chip	Need
L (nH)/R_{DC} (mΩ)	15-25	5-10	0.1-0.2	>>10
Q	>20	<10	5	>20
Current (A/mm^2) Thickness	0.01 – 0.1 200- 500 µm	0.1 – 1 50 - 200 µm	5-10 A/mm^2 25 µm	5-10 A/mm^2 25-50 µm core
Cost	Low	Low	High	Low
	Discrete - Example (0.5 x 0.1 x 0.5 mm) 	  Substrate-embedded inductors Magnetic Core (0.5 - 0.6 mm)	  Intel and Ferric	

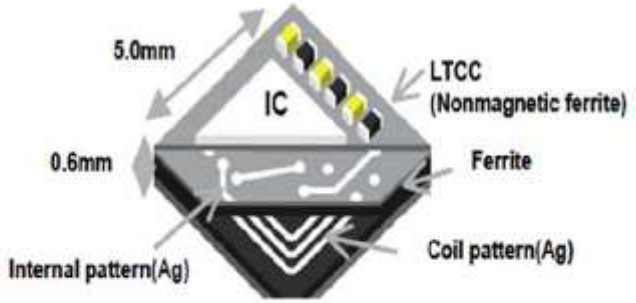
Magnetic Material Options

	Thickness Microns	Coercivity A/m	Resistivity μ Ohm cm	Saturation Flux (Tesla)	Permeability
Mn,Zn ferrites	>100	3-5	10,000	0.6	5000
Nanocrystalline and amorphous flakes	>15	3	110	1.2	15000
0.1 – 5 MHz					
Electroless thinfilms	3-5	10-20	100	1	<<1000
Plated thin films	2-100	20-80	35	1.3	~1000
Flake composites	25-500	100-200	10,000	0.8	100-150
1 – 10 MHz					
Nanomagnetic films	1-10	10	200-300	1.5	200-500
10 – 150 MHz					

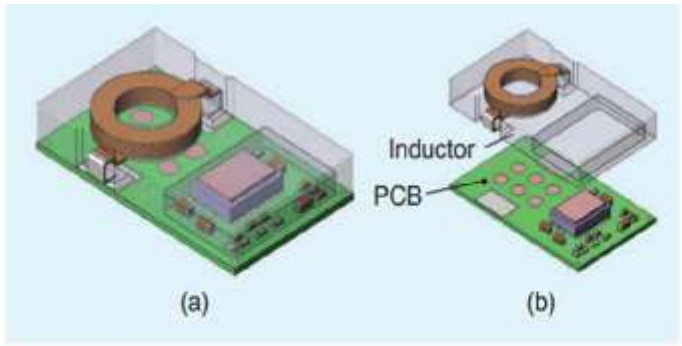
Integrated Inductors

- Small footprint (0201 – 0.2mm x 0.1mm) discrete inductors, using high frequency (100MHz+) polymer loaded composites or fired magnetic material. Surface-mount devices [Murata] or with copper terminations, embedded in the SOC organic substrate or package [Taiyo Yuden].
- High frequency ferrite cores embedded in 2.5D/3D heterogeneous integration structure using BEOL interconnect processing to provide windings [IMEC].
- Vertical coaxial magnetic composite core inductors integrated in the package substrate [Intel].
- Embedded magnetic-on-silicon inductors embedded in PCB substrate or package [Wurth].
- Embedded thin film CZT combined with copper windings in PCB substrate or package [Tyndall].
- Electroplated planar copper windings with electro-deposited magnetic core [Enachip].
- Vertical inductors based on thin film CZT deposited on the sidewalls of low-profile electroplated copper pillars [Tyndall].

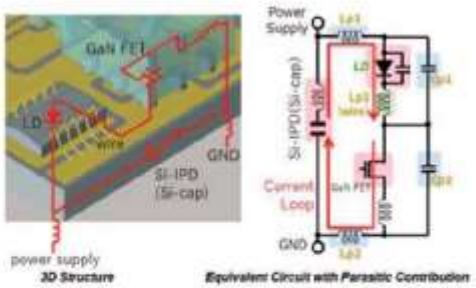
Embedded Inductors in Power Modules



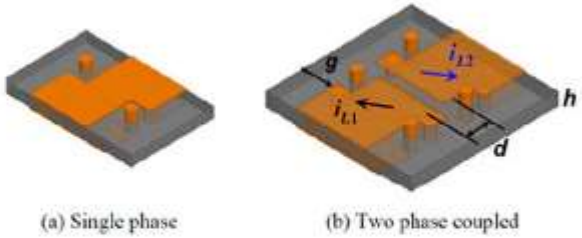
Murata, Ferrite and LTCC Inductor substrates



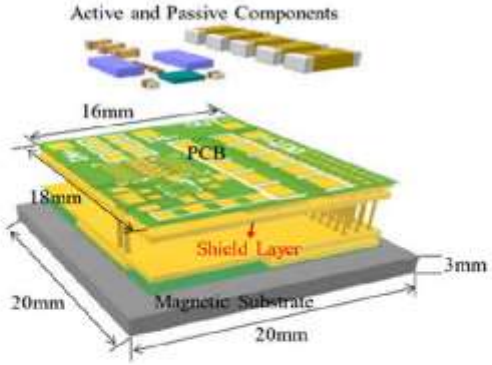
Sumida
(Inductors in lead-frame molding)



Modules on silicon capacitor substrates;
Murata's LIDAR modules



Virginia Tech
(Inductors in laminate)

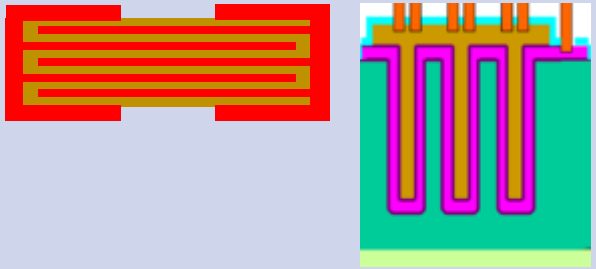


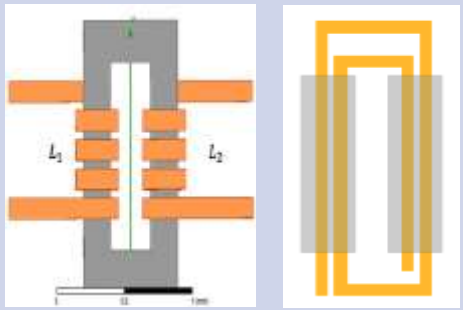
GaN DC-DC converter with substrates-embedded inductors

Key R&D for IVR Inductors

- Requires considerations of 3D inductor design, magnetic material synthesis and processing, integration and assembly into packages, substrates and interposers.
- Increasing DC nH/mOhm beyond 1.0 (up to 5.0 to 10.0).
- For magnetic core solutions, increasing the saturation current up to 5 to 10 A DC.
- Exploiting the vertical direction to provide reduced footprint, ultra-low dc resistance inductors – to produce a useful, single vertical inductor.
- Exploring integrated inductor arrays in interposers or substrates for complex granular power architectures.
- Considering the EMI implications of integrated inductors and appropriate solutions.
- Utilizing the “parasitic inductances” within the system architecture, either with or without magnetic material enhancements.

R&D Needs for Passives

Capacitors 	Density	High K dielectrics; Enhance electrode surface area; New dielectrics and deposition processes
	Frequency stability	Electrodes and connectivity with lower parasitics
	Integration	Thinner form-factors; Substrate or wafer or fan-out embedding

Inductors 	Density	Higher permeability with saturation field and high resistivity
	Efficiency	Low coil DC losses ; Low core losses with low coercivity and eddy currents
	Integration	Substrate- or wafer-compatible process
	Current-handling	Design innovations; Scalability in thickness to handle higher current

Integrated Power Electronics Technical Working Group

Many Thanks For Your Attention

If interested in joining our IPE-TWG please contact any of our members.