3D-PEIM
International Symposium on 3D Power Electronics Integration and Manufacturing

Enabling Sustainable Power Electronics Through Miniaturization and Integration of Power Magnetics

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VP Engineering & Magnetics – EnaChip Inc.

The Problem:

World needs

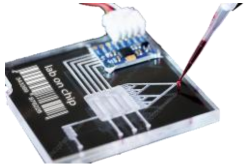
MORE power in SMALLER spaces:

High Power Density

Concentrated Functionality

Electrification - Autonomy

Advanced Health



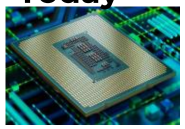
Aerospace - Defense

Computing

90's

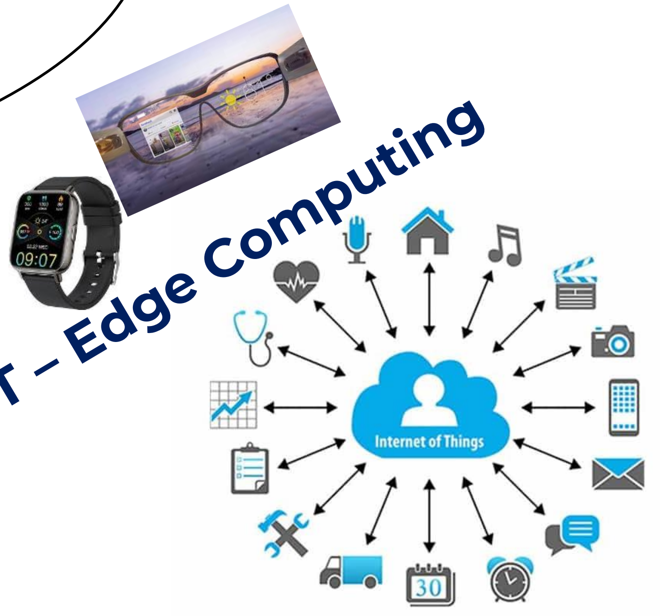
3 million transistors

Today



7 billion transistors

IoT – Edge Computing



Breaking Down the Problem

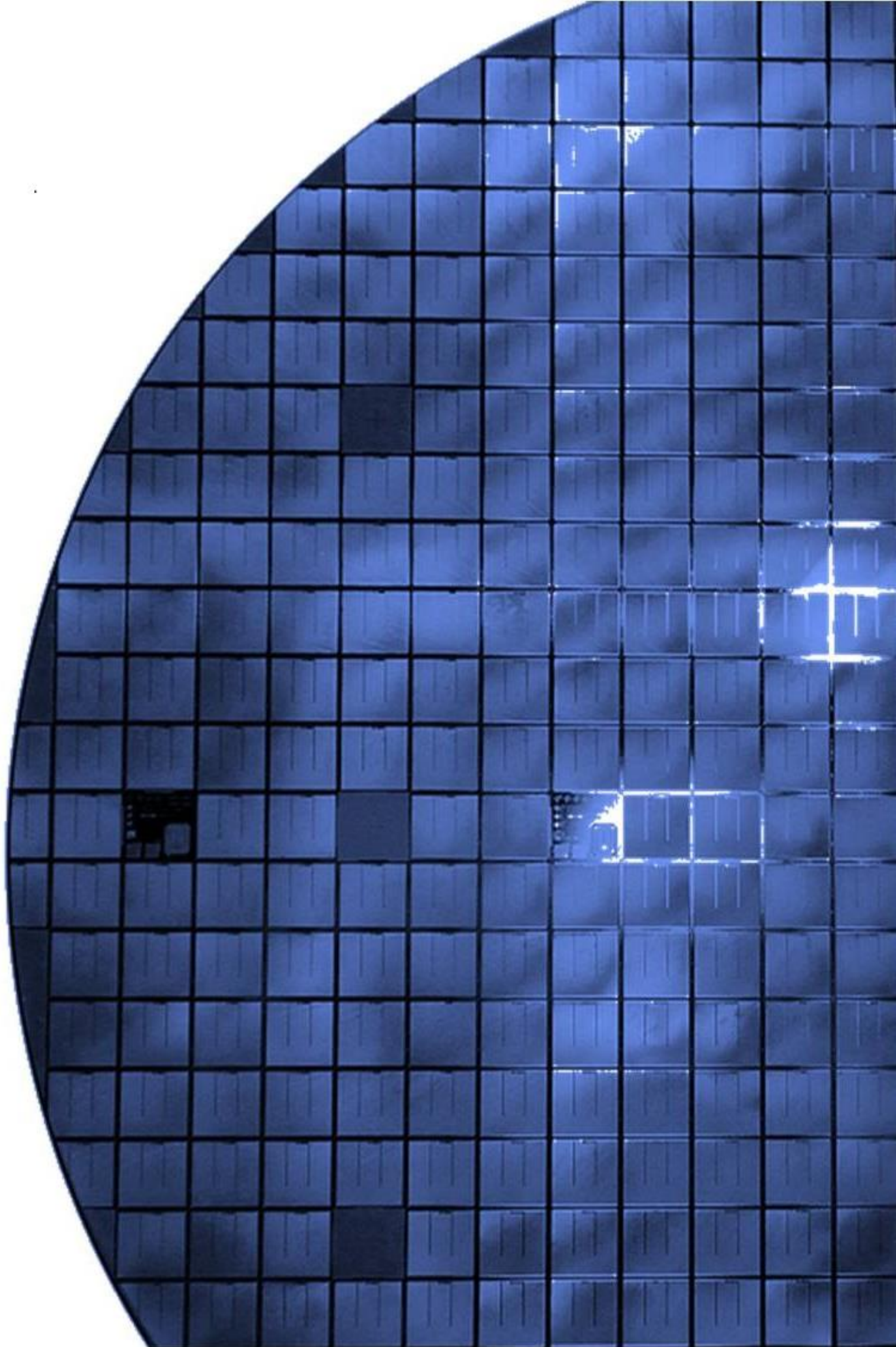
- New megatrends like AI, and the age of “Everything Connected” continue to drive power needs for higher performance computing, mobility, connectivity and autonomy.
- Electronic devices and applications continue to push the boundaries of size – smaller and more compact form factors, ultra-high speed data transmission, and improved energy efficiency.
- Proposed solutions must feature the ease of design, integration into an existing ecosystem and minimal re-learning for developers.
- Legacy technologies are not enough!

  these multitudes of new and emerging applications require a re-imagined solution space for design of electronic devices including microchip power solutions

S	*size*
W	*weight*
A	*and*
P	*performance*
C	*cost*

– THE ROOT CAUSE of
POWER INEFFICIENCIES

Power
Is Separate From
Silicon

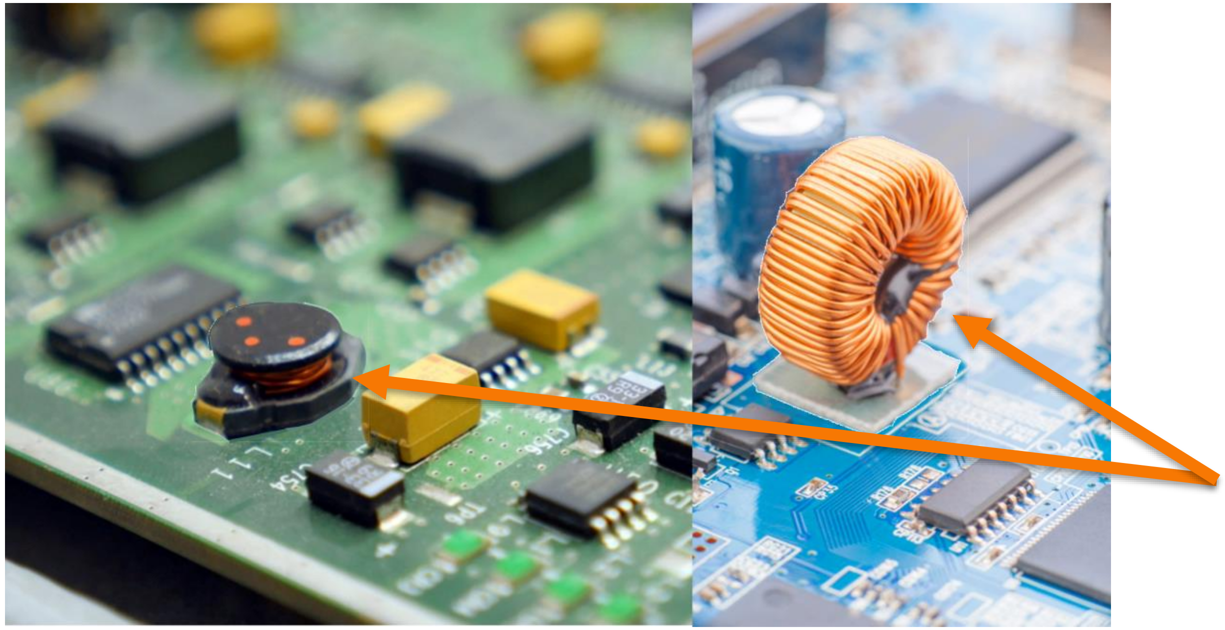


Required Fundamental Magnetics Solution

Leading edge magnetic materials and device designs to provide a **solution space that is a customizable convergence of performance and desired form factors** for even the most demanding electronic applications in computing, mobility, power and sensing.

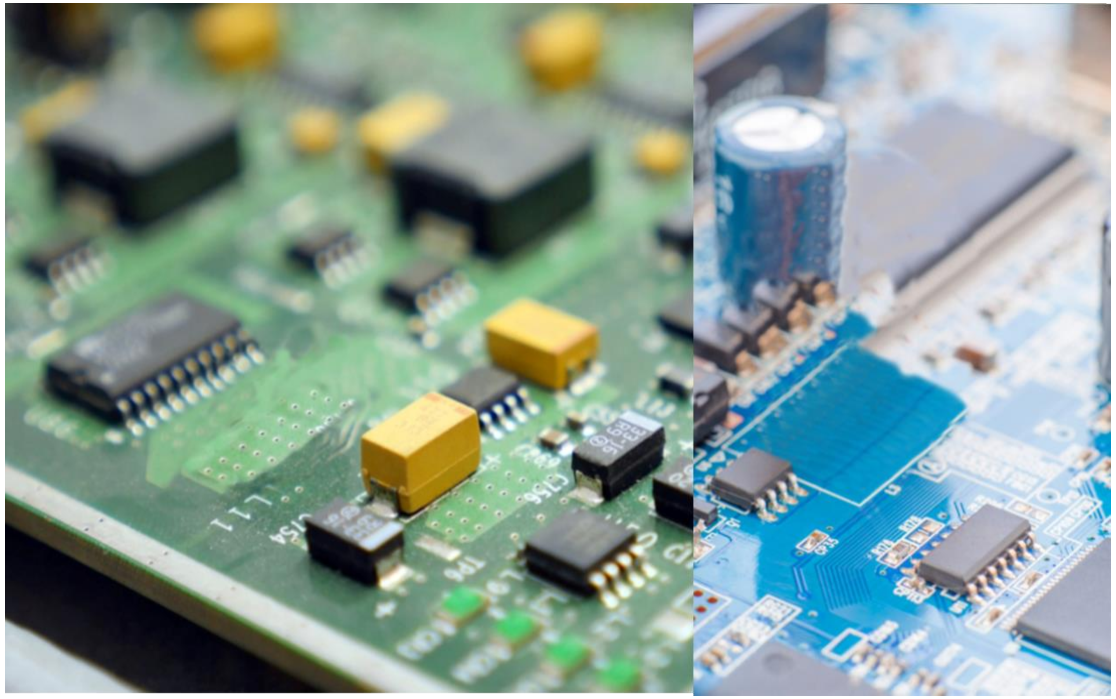
Basic ingredients include:

- **Low cost** of implementation
- **Ecosystem** in place
- Seamlessly **Integratable** into market driven devices



INTEGRATION ROADBLOCK

Discrete power magnetics
(e.g., Inductors and transformers)
are the largest components on the board!



Wafer Level Magnetics Integration will make them invisible!

Goals of Magnetics Integration

Meet cost – manufacturing and packaging

Meet form factor – footprint and thickness

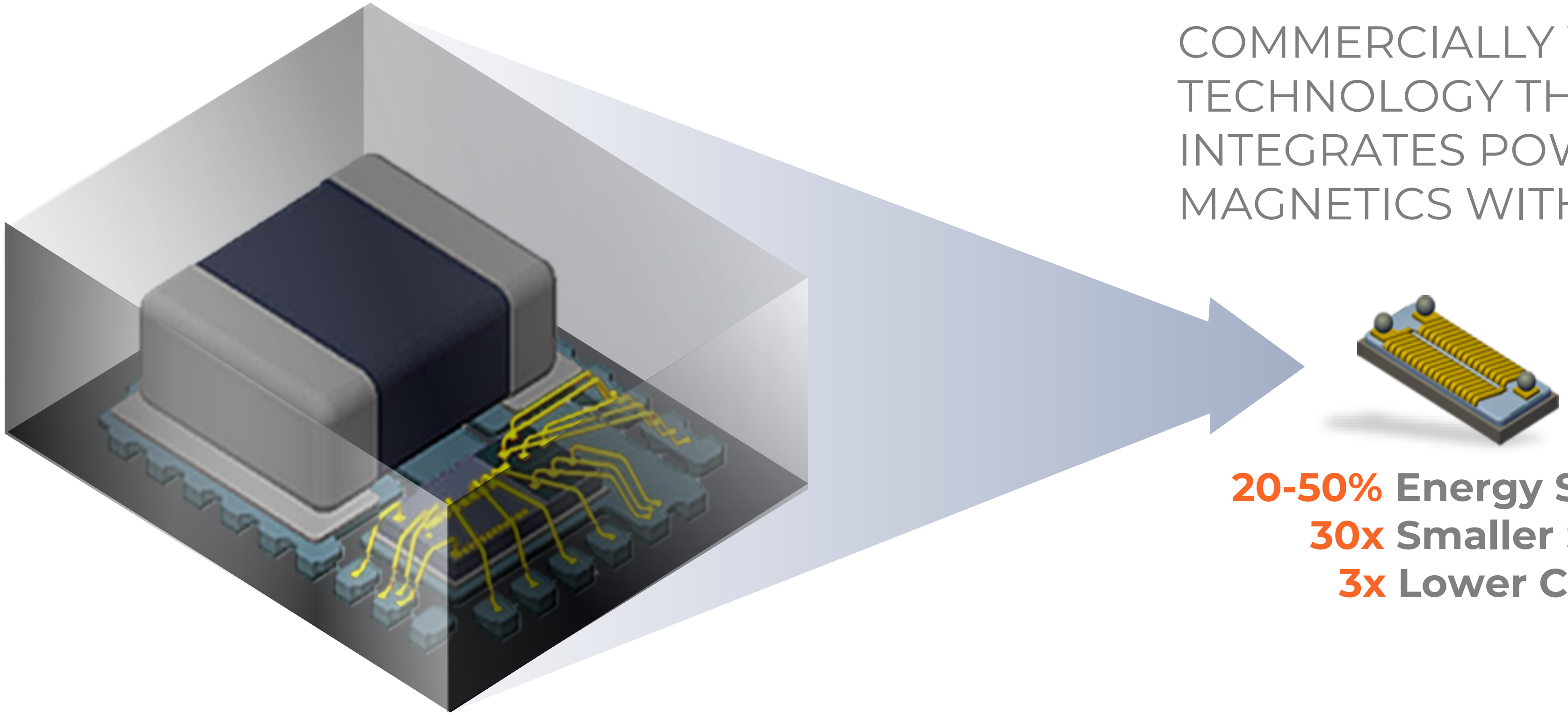
Meet quality and reliability

Meet performance - electrical I_{SAT} - L - DCR - Q (Power Loss)

The intangibles – near field noise, thermals, integration compatibility

Wafer Level Magnetics is a viable option to meet these goals

Wafer Level Magnetics
Next Step For Innovation in Integration



COMMERCIALLY VIABLE TECHNOLOGY THAT INTEGRATES POWER MAGNETICS WITH SILICON IC

20-50% Energy Savings
30x Smaller Size
3x Lower Cost

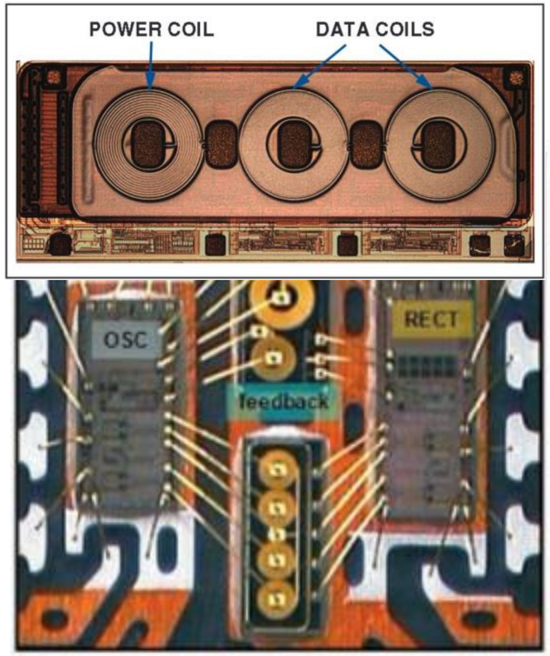
Power System in Package

Power System on Chip
EnaChip Enabled Solution

Wafer Level Magnetics

(Core technology options)

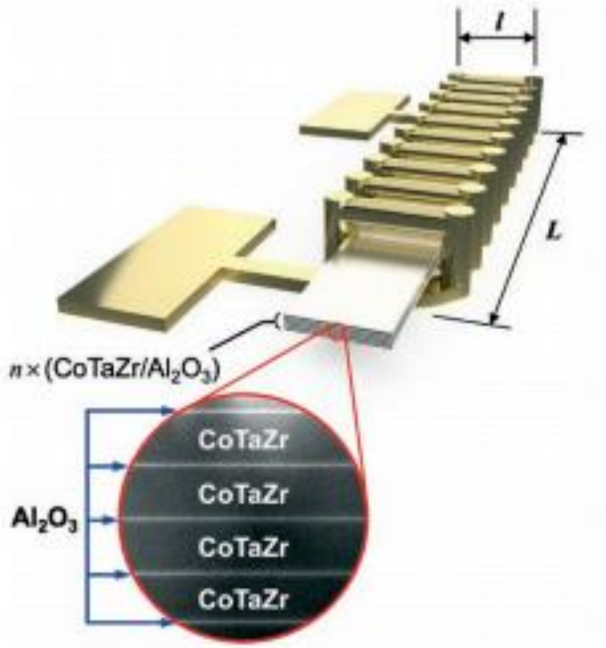
Aircore WLM



iCoupler, ADI

Electroplating windings

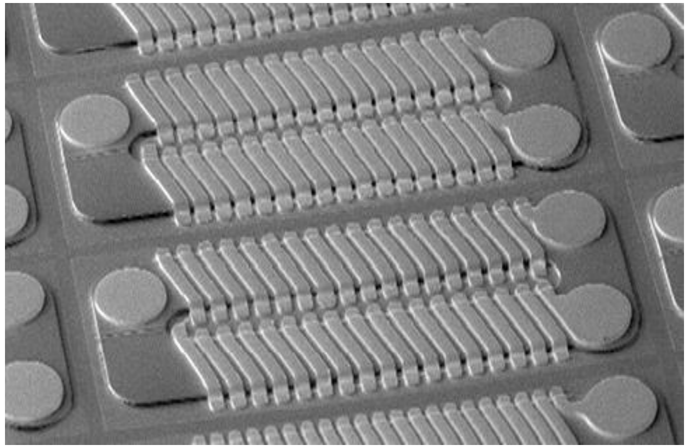
Multilayered thick film sputtered core



Evatec

Electroplating windings

Multilayered thick film electroplated core



Enpirion

Electroplating windings

Wafer Level Magnetics

(Core technology comparison)

Aircore WLM

- ⬆ Easy to fabricate
- ⬆ Low cost
- ⬆ Low power loss
- ⬇ High near magnetic fields
- ⬇ Low inductance
- ⬇ Requires high F_{sw}

Multilayered thick film <u>sputtered</u> core

- ⬆ High performance
- ⬆ Process/thickness control
- ⬆ FEOL compatible
- ⬇ Slow (0.1um/min)
- ⬇ High cost process (~10-20x of the plating)
- ⬇ High capital costs (>5X over electroplating)
- ⬇ Thickness/Stress limitations (<20L, <3 um)

  Power ≈ core thickness

Multilayer thick film <u>electroplated</u> core

- ⬆ Fast deposition (1um/min)
- ⬆ Low cost process
- ⬆ Intrinsically low stress

  → No. layers (>100)
- ⬆ Low capital costs (BEOL-OSAT)
- ⬆ Highly scalable
- ⬇ Metallic high μ crystalline films have low ρ→ small skin depth → higher loss
- ⬇ Multi-layer laminations needed for high currents >1A

  Complex multi-layer/multi-mask **cost prohibited process**

Enachip’s Technology Platform

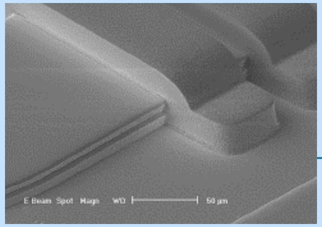
Enachip addresses the electroplating core shortcomings to enable a high performance WLM cost competitive solution

Electroplating core

- ↑ Fast deposition process (1mm/min)
- ↑ Low-cost process
- ↑ Intrinsically low stress → No. layers (>100)
- ↑ Low capital costs (BEOL - OSAT)
- ↑ Highly scalable
- ↓ Metallic high μ crystalline films have low ρ→ small skin depth → higher loss
- ↓ Multi-layer laminations needed for high currents >1A

  Complex multi-layer/multi-mask **cost prohibited process**

EnaChip Creates an Enabling Technology Platform



Unique high-performance magnetic materials

Innovative wafer fabrication processes

+

silicon based control circuits
(node independent)

Multiple Addressable Market Verticals

Intelligent Sensors - Automotive and IoT
- Current sensing
- Magnetic Field Sensing

Connected and Smart Health
- Electromagnetic Separation
- Micro-*pumps, micro valves, relays*

Microdevices
Electromagnetic Actuators
Power Harvesting
Switches

Current Roadmap Focus

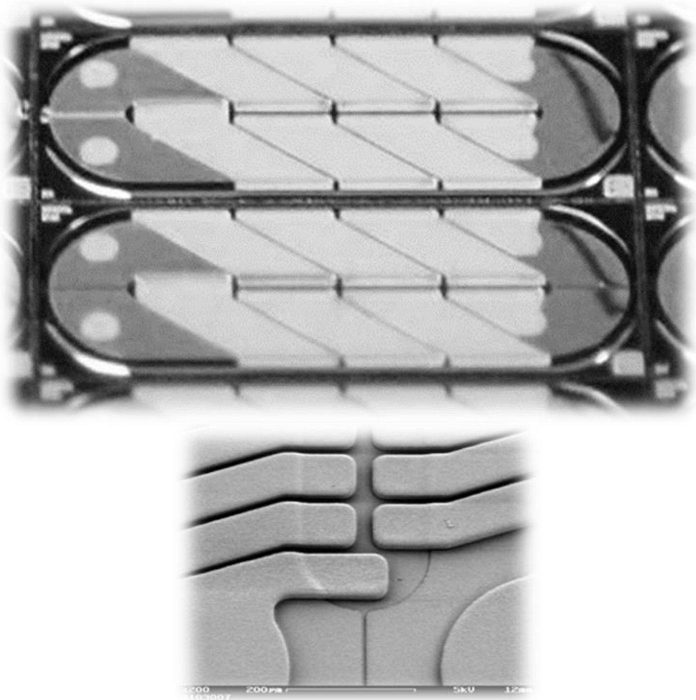
Power Management
DC/DC Voltage Regulators
PMIC
LED Drivers

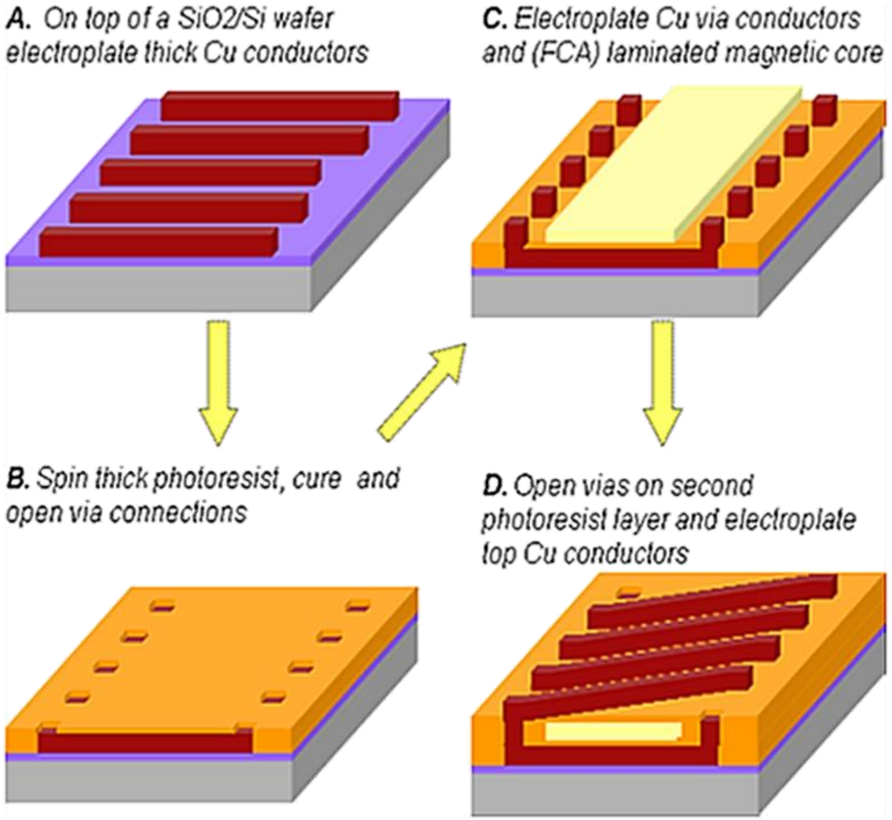
Signal Conditioning
Filters
Tuners

Key Process Modules

(Electroplated micro-coils)

- Thick electroplated Cu (5um – 80um)
- Dielectric insulation/planarization
- Electroplated high frequency magnetic alloy laminations





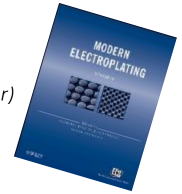
A. On top of a SiO2/Si wafer electroplate thick Cu conductors

B. Spin thick photoresist, cure and open via connections

C. Electroplate Cu via conductors and (FCA) laminated magnetic core

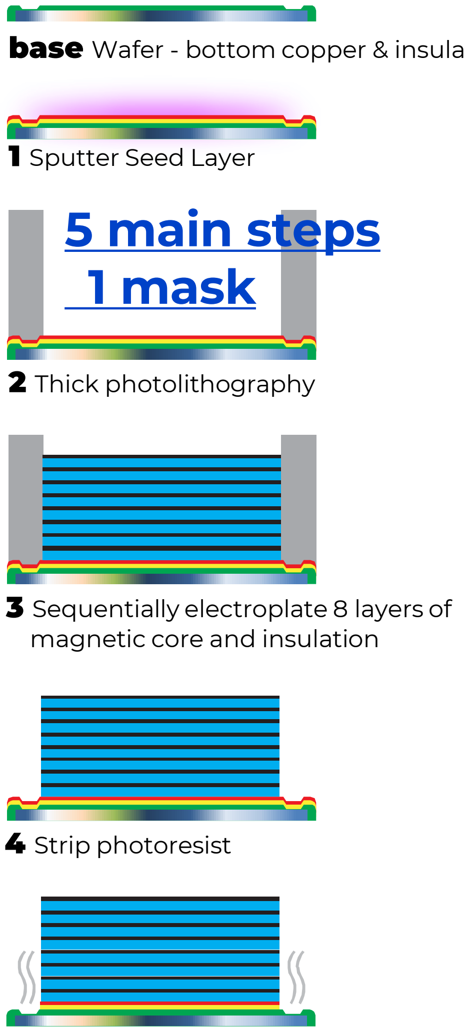
D. Open vias on second photoresist layer and electroplate top Cu conductors

Ref. Modern Electroplating, 5th edition
Mordechay Schlesinger (Editor), Milan Paunovic (Editor)



Game Changing Cost Reduction !

EnaChip process for 8 core layers
Using **electroplated EPI** as insulator



base Wafer - bottom copper & insulation

1 Sputter Seed Layer

5 main steps
1 mask

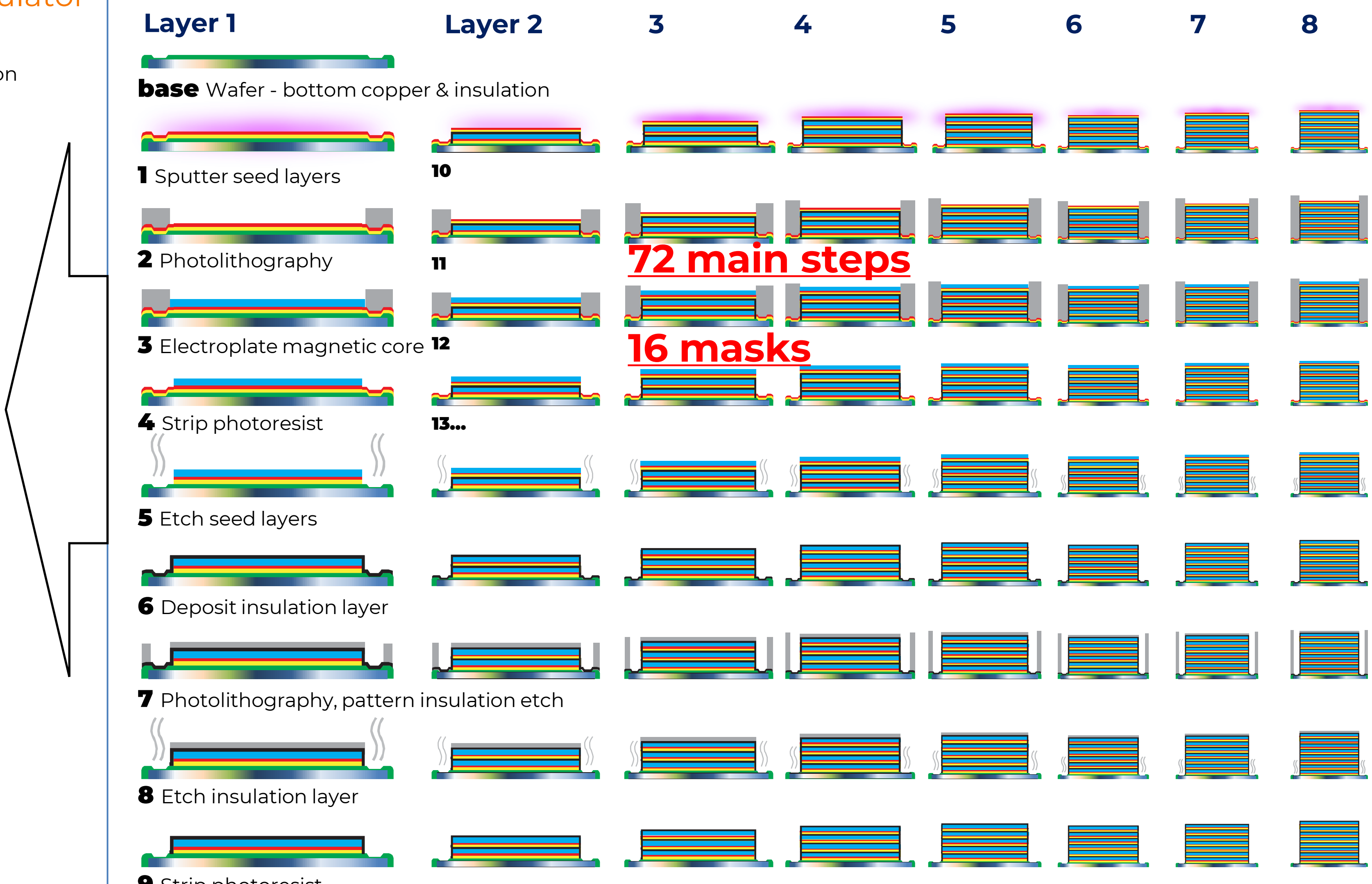
2 Thick photolithography

3 Sequentially electroplate 8 layers of magnetic core and insulation

4 Strip photoresist

5 Etch seed layers

Today's process for 8 core layers using **sputtered SiO_2** as insulation



base Wafer - bottom copper & insulation

1 Sputter seed layers

2 Photolithography

72 main steps

3 Electroplate magnetic core

16 masks

4 Strip photoresist

5 Etch seed layers

6 Deposit insulation layer

7 Photolithography, pattern insulation etch

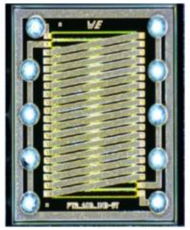
8 Etch insulation layer

9 Strip photoresist

Electroplating's Competitive Advantage

Sputtered Laminated Cores

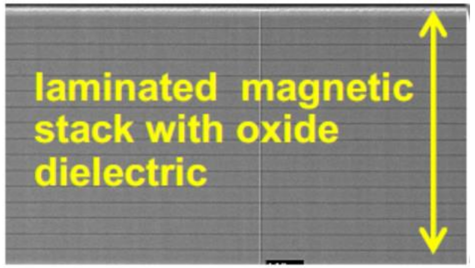
- **High Cost**
- **Slow process**
- **Foundry node bound**



Microtransformer
(2.6mm x 2.4mm)

20L TOTAL 4.5um

Deposition time 1.6 days !



(up to 5um)

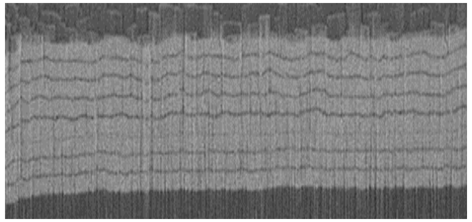
Continuously Electroplated Laminated Cores

- **Simple process**
- **Ultra Low Cost**
- **Ultra fast process**
- **On Any wafer, Any Node!**

Microtransformer
(1.7mm x 4.0mm)

8L TOTAL 8um

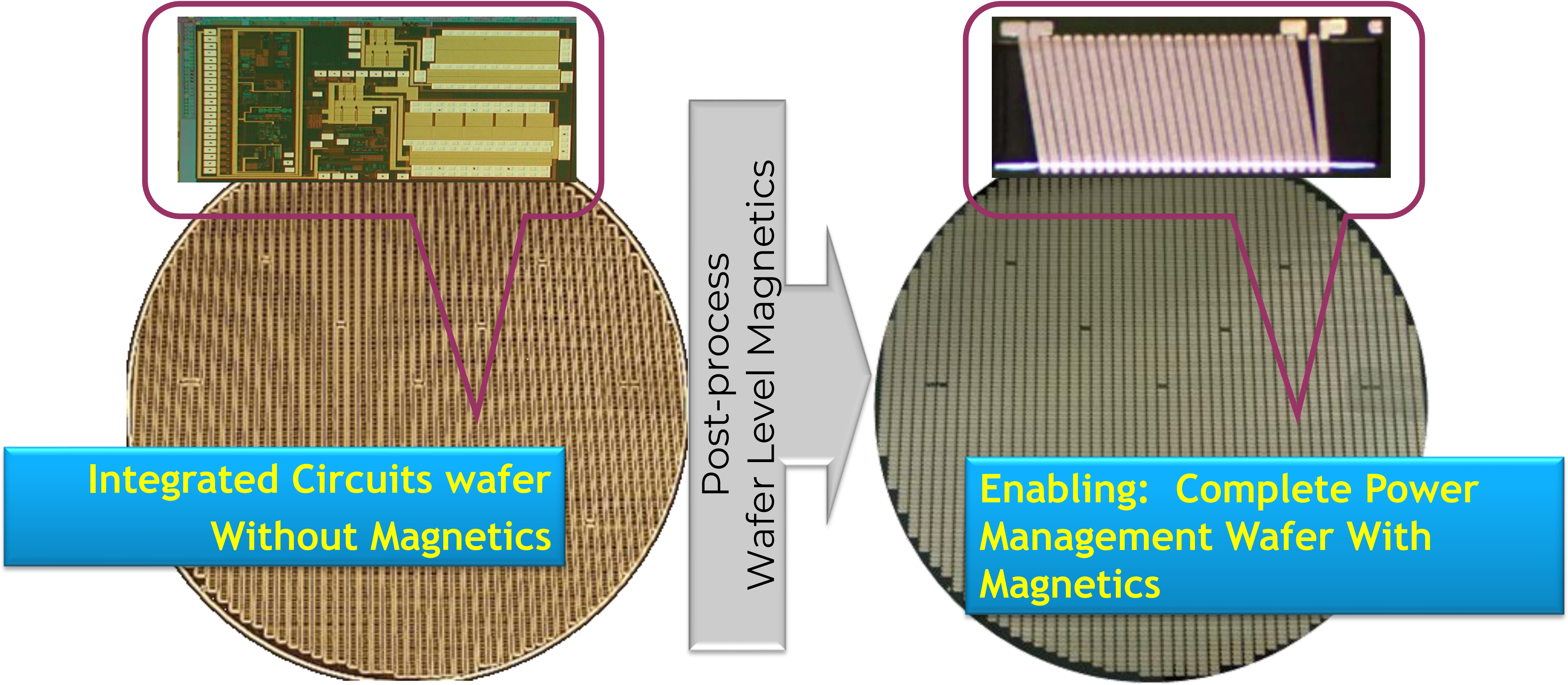
Deposition time 1.2 hours !



(no limits)

The advantage of being… Node-Agnostic

(EnaChip's "Magnetic Functionality" can be post-processed on ***ANY substrate*** *from* ***ANY foundry*** *and* ***ANY node!)***



Controller+PFETs wafer

Wafer Level Magnetics post processed wafer

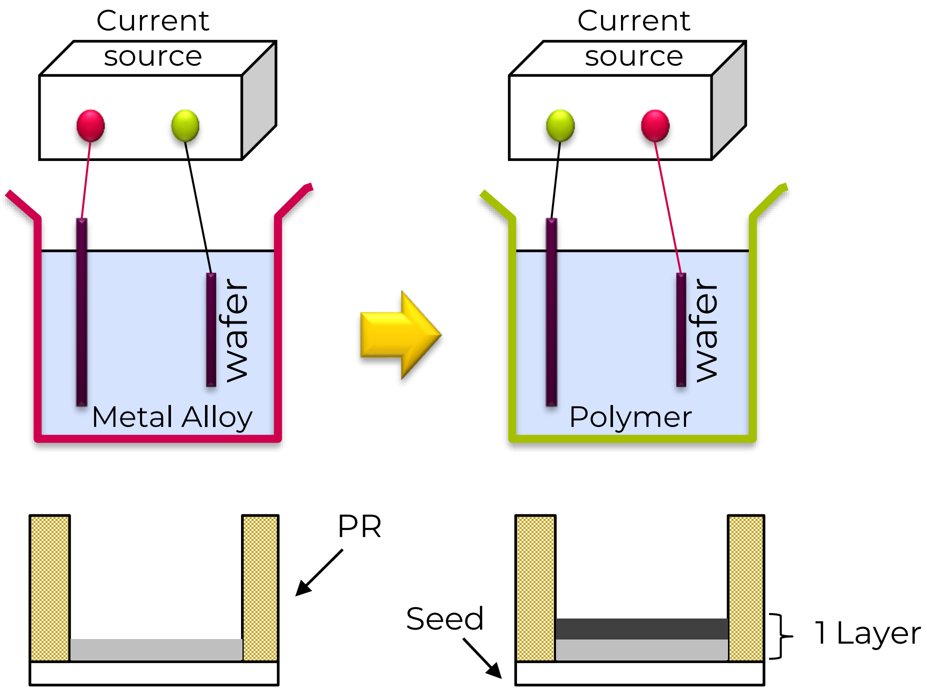
Post-process Wafer Level Magnetics

Integrated Circuits wafer Without Magnetics

Enabling: Complete Power Management Wafer With Magnetics

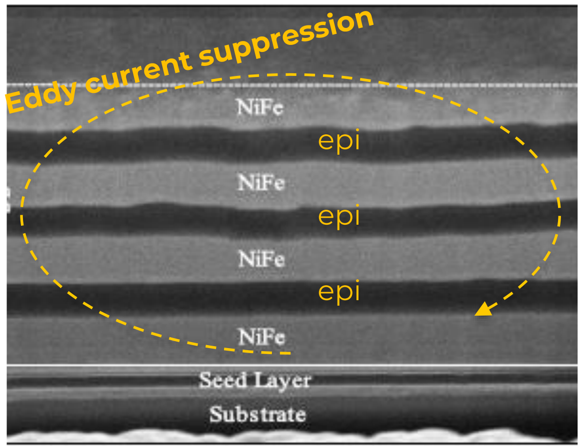
Multi Layer Process Incorporates Electro Plated Insulator (EPI)

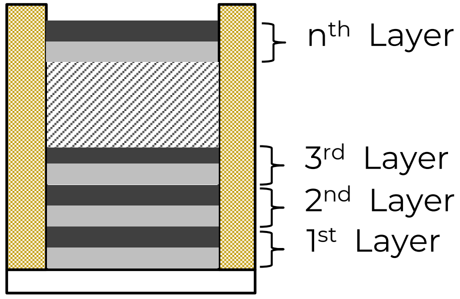
- Electrochemically synthesized insulator
  - – Conjugated polymer based
- Conductivity < 1S/m



× n →

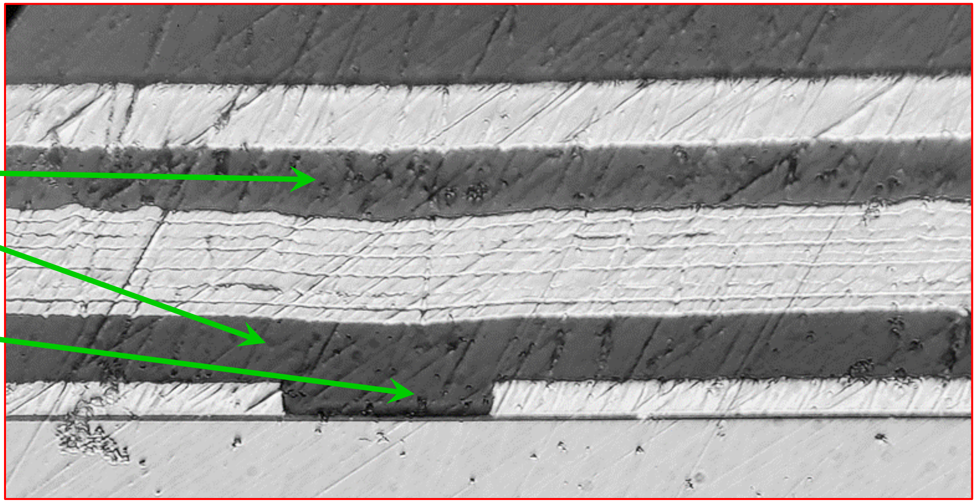
For n-layer core Device

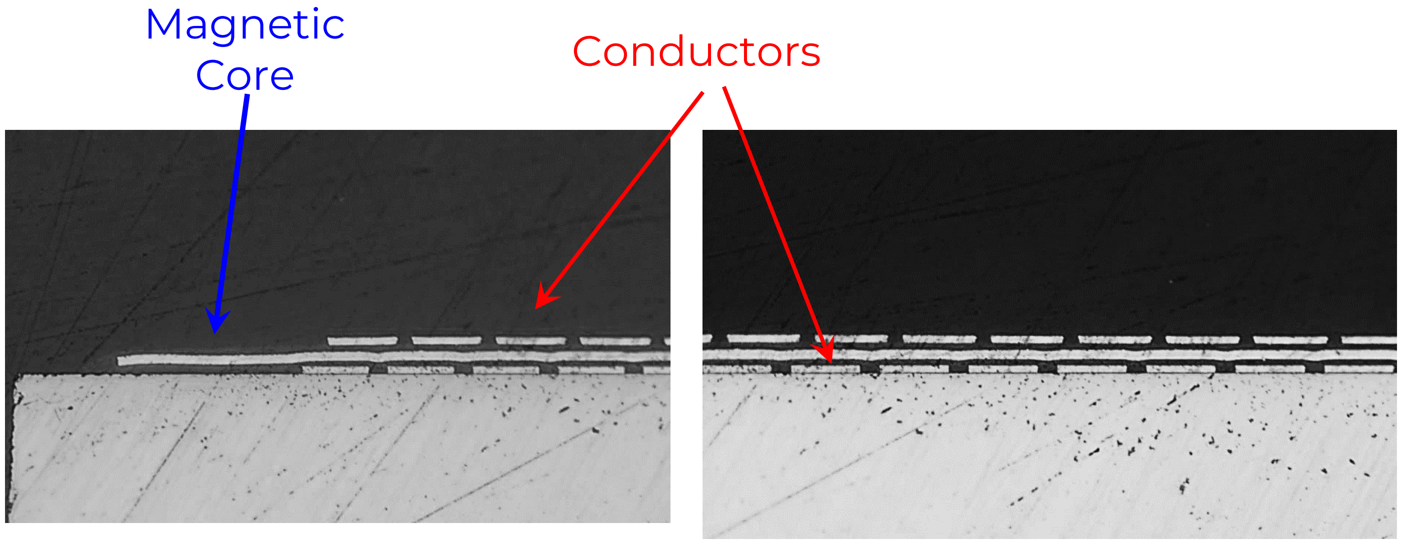


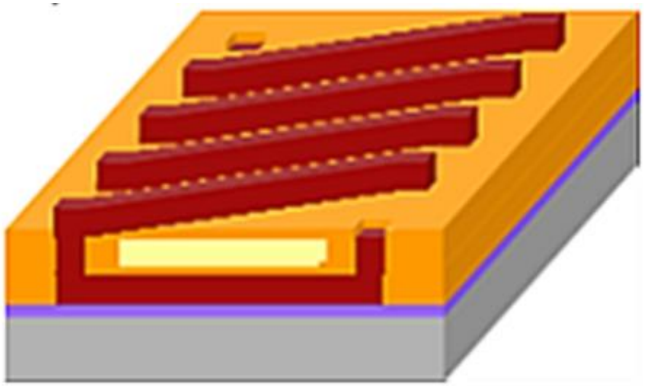


Photolithographically definable dielectric

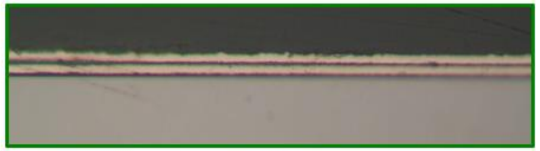
- Photosensitive cured polymer as dielectric
  - Between magnetic stack and conductors
  - Between conductors
- Dielectric Constant ~ 4
- Breakdown Voltage > 600 V/mm



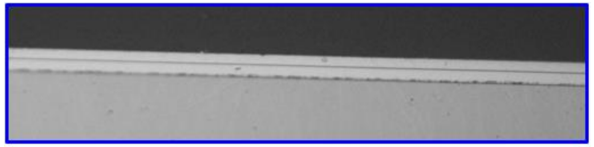




EnaChip's Electro-Plated Insulation "EPI"
(Performance comparison of EPI vs. SiO$_2$ as lamination insulator)

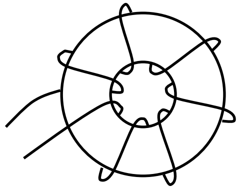


ECA
2 Layers
3 um/Layer
EPI Between Layers



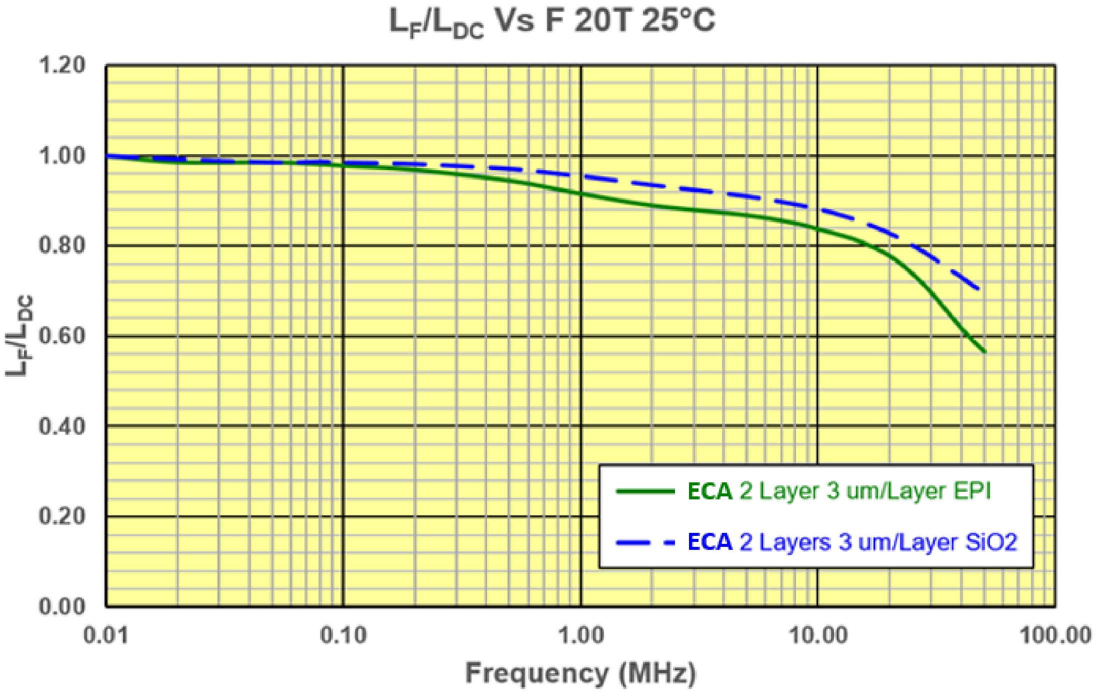
ECA
2 Layers
3 um/Layer
SiO$_2$ Between Layers

Test donuts are made of 2 Layers of magnetic material separated by EPI and SiO2 for comparison



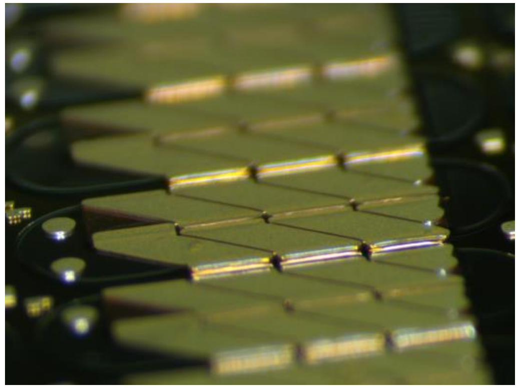
- Donut-0 ID=6mm OD=19mm
- Closed magnetic path

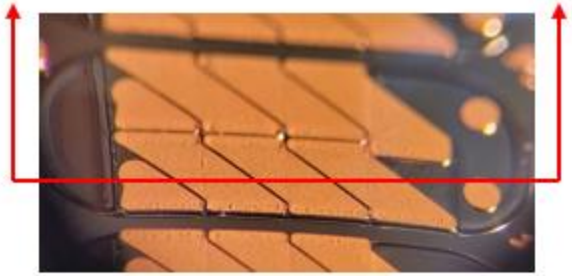
EPI insulation is as good as SiO2 insulation

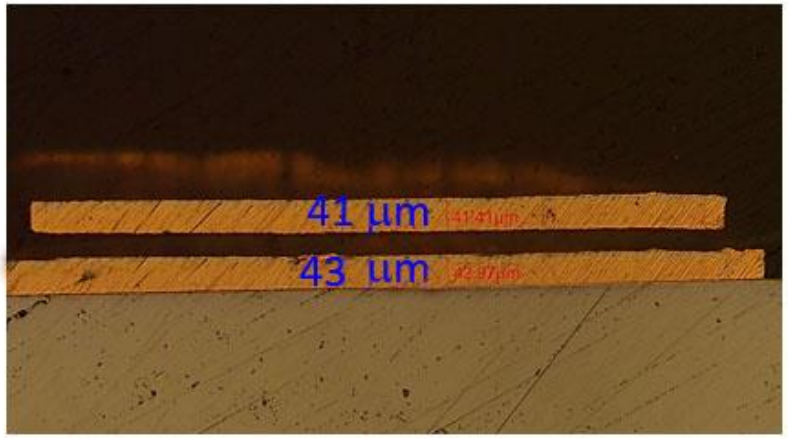


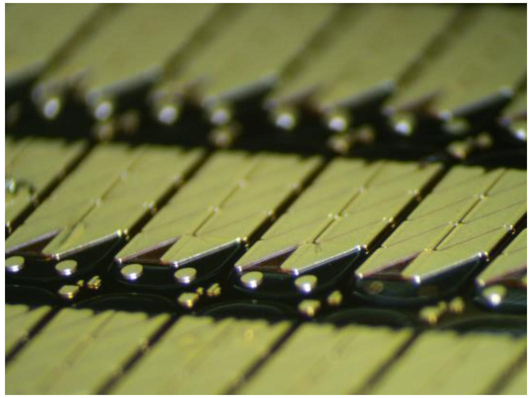
Thick (> 40 µm) Copper

- Thick copper enables lower DCR per turn
- For a given DC power loss budget
  - Lower DCR per turn enables more turns
  - More turns enables higher value of inductance
  - More turns enables higher volt-second capability
- Higher values of inductance and volt second capability
  - Enable higher input voltage buses beyond 3.3V, 5V, 12V towards 18V/24V

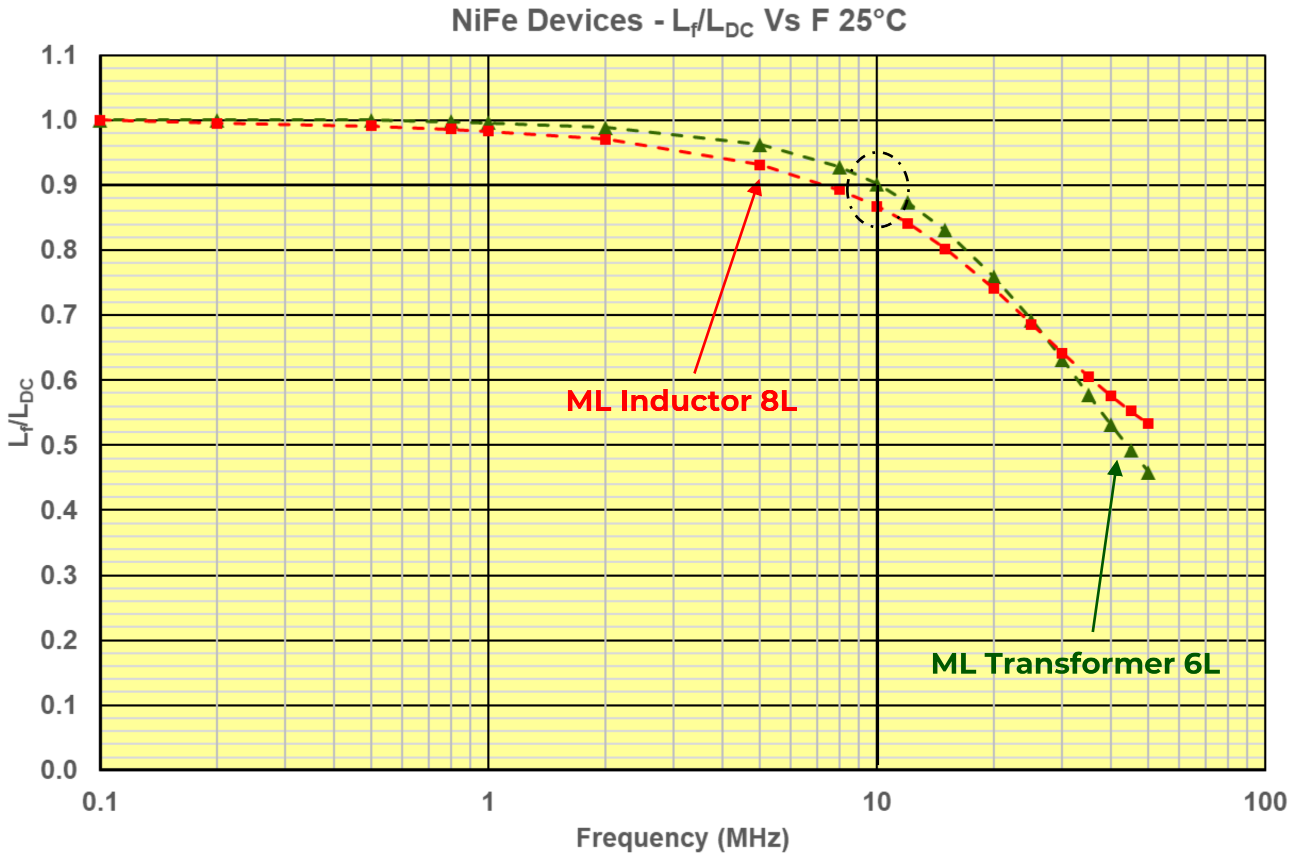




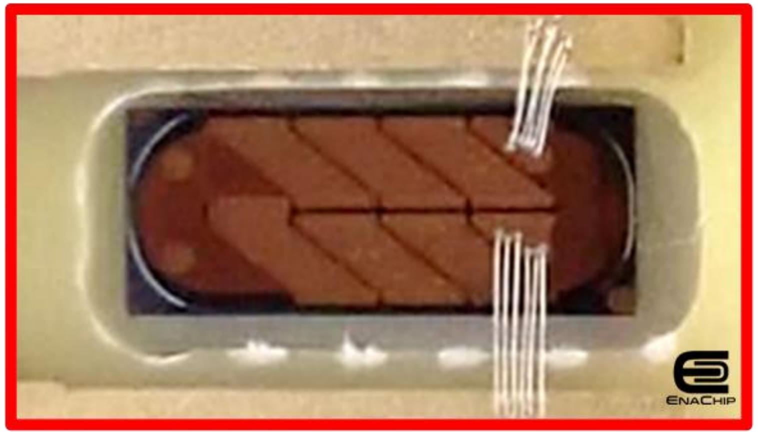




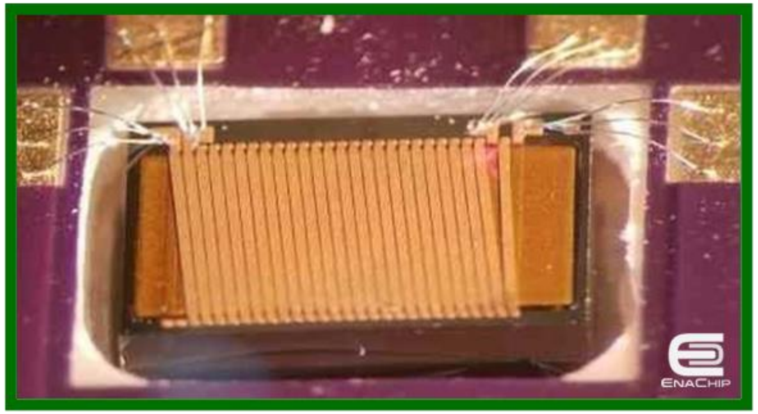
Device Performance
Using Mag Core with Single Mask n-Layer process



EnaChip multilayer lamination process extends the performance of NiFe materials
to maintain higher values of inductance at higher frequencies.

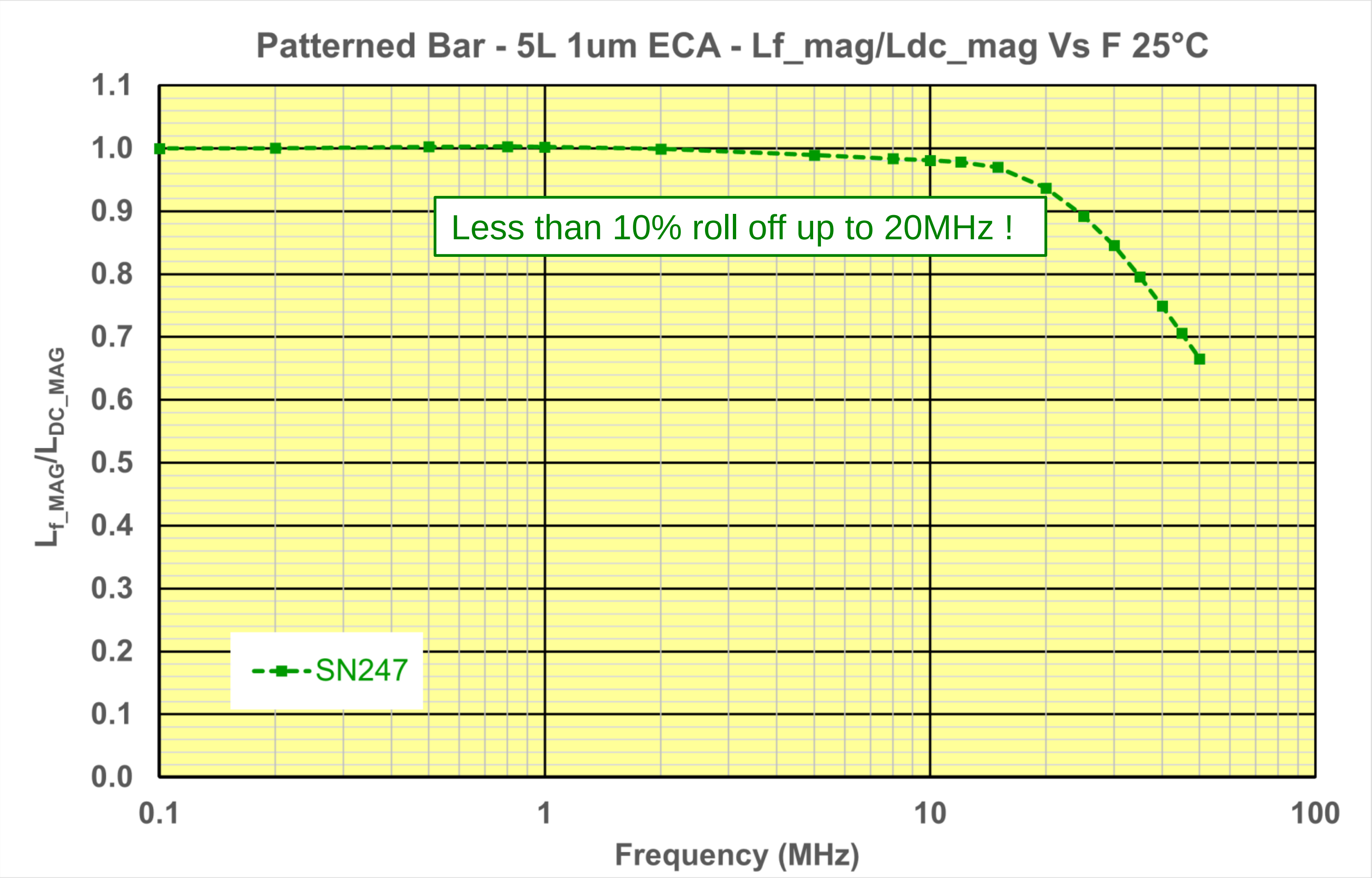


L=20-40nH die 2mm x 5mm



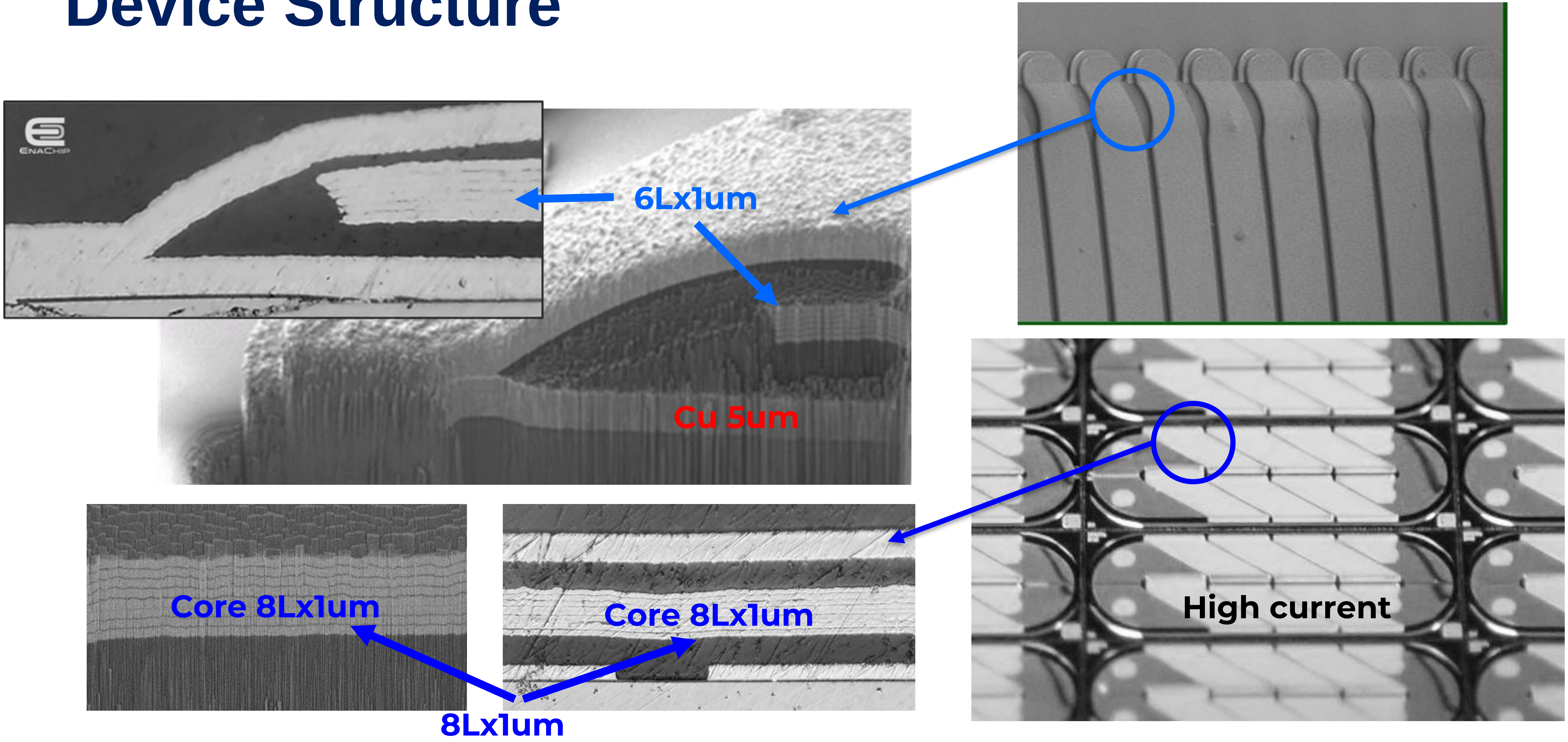
L=120-150nH die 1.7mm x 4.0mm

Multi Layer ECA – High Frequency Performance

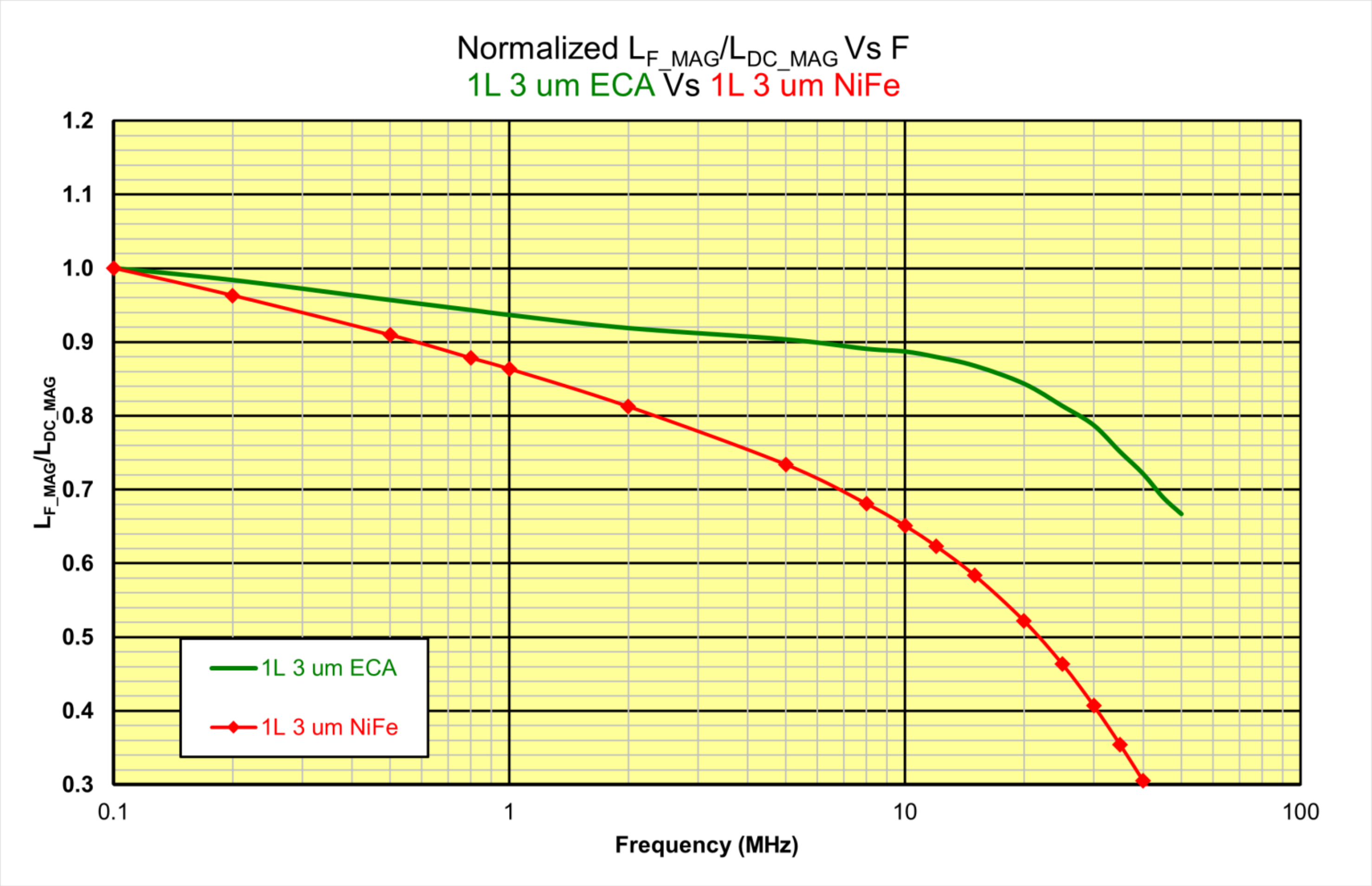


EnaChip Inc. presented at 3D PEIM 2023

Device Structure



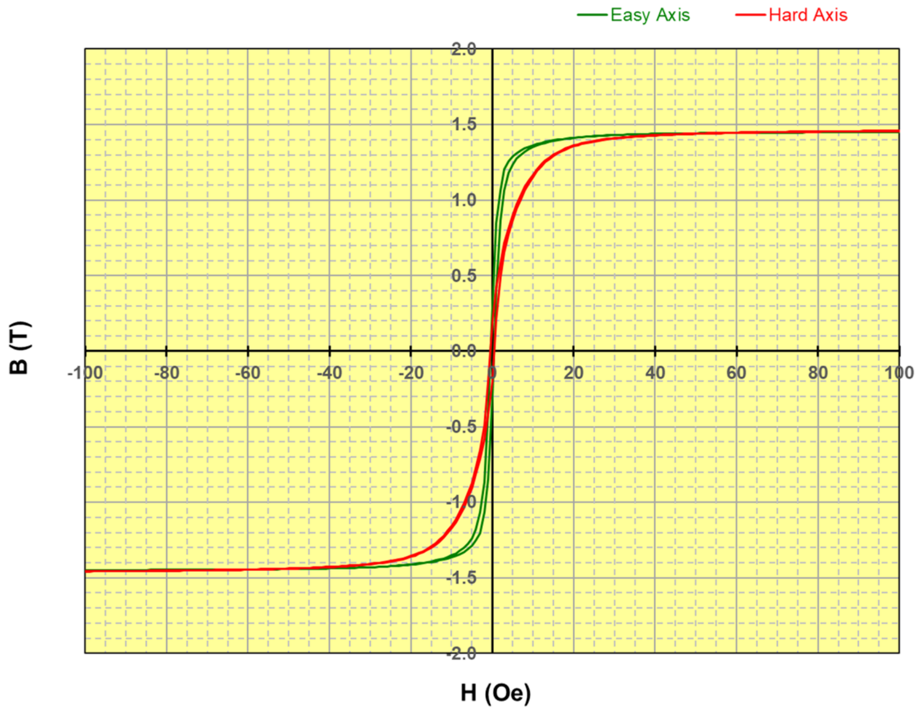
EnaChip's alloy ECA vs. NiFe



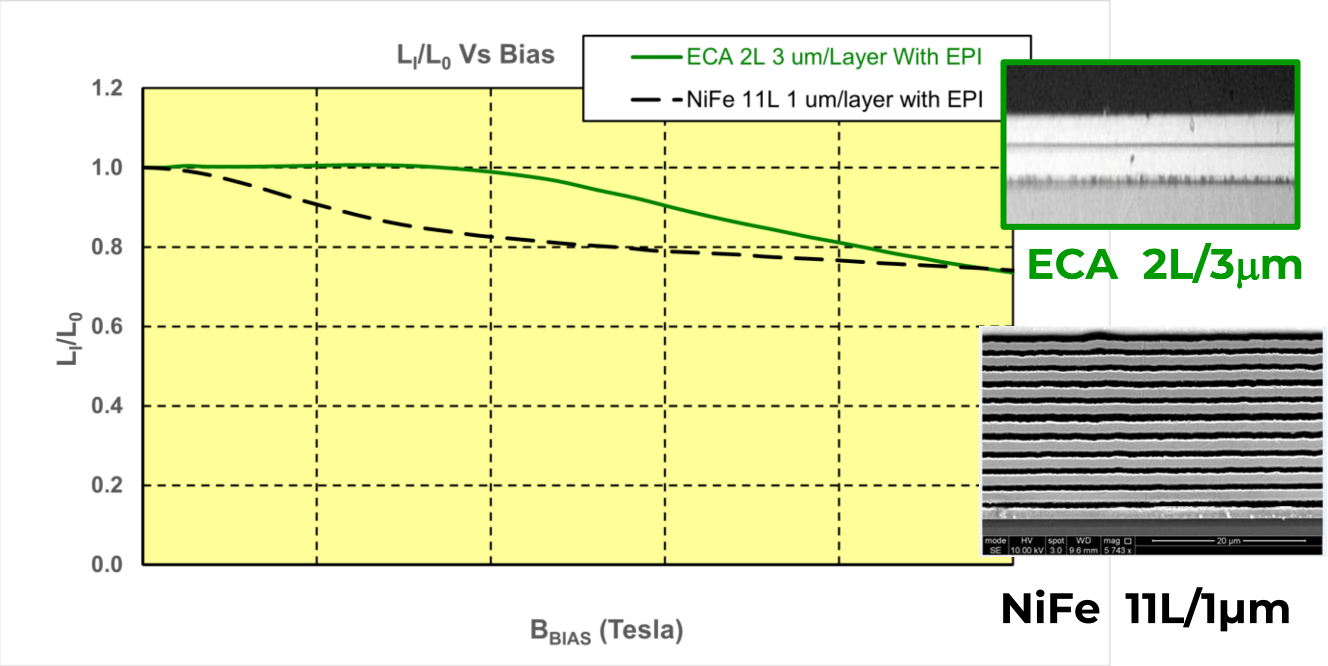
High Performance Proprietary ECA Alloy

Ena**C**hip **A**lloy (**ECA**)

  - Permeability up to 900
  - $B_{sat} \geq 1.5$ T

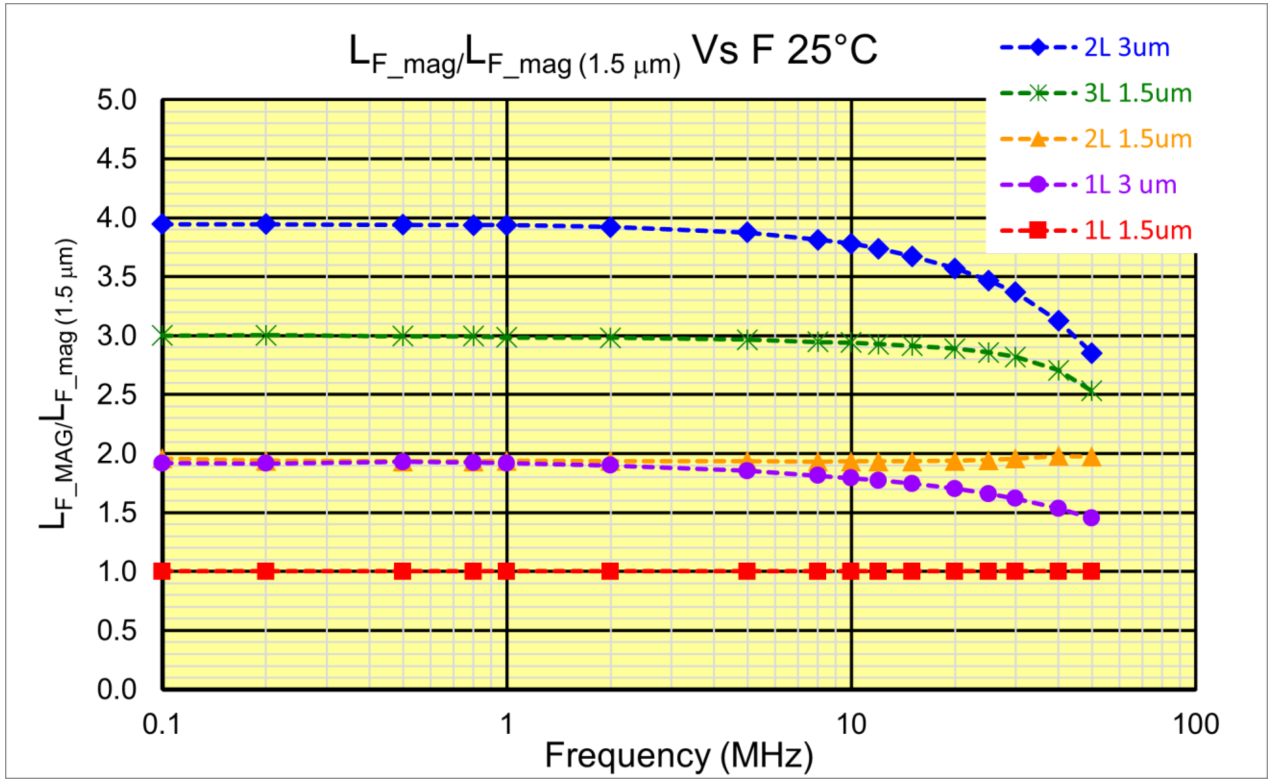


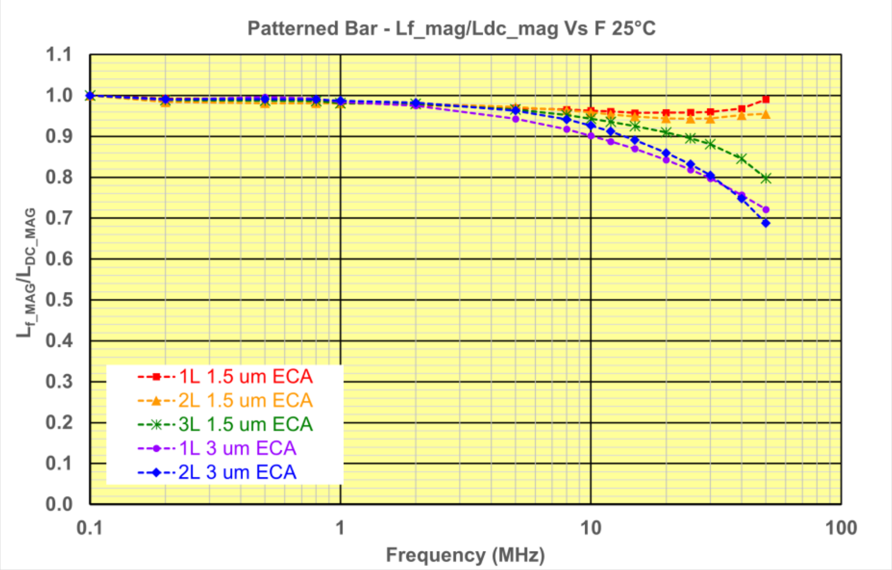
ECA Bias operational range >> NiFe

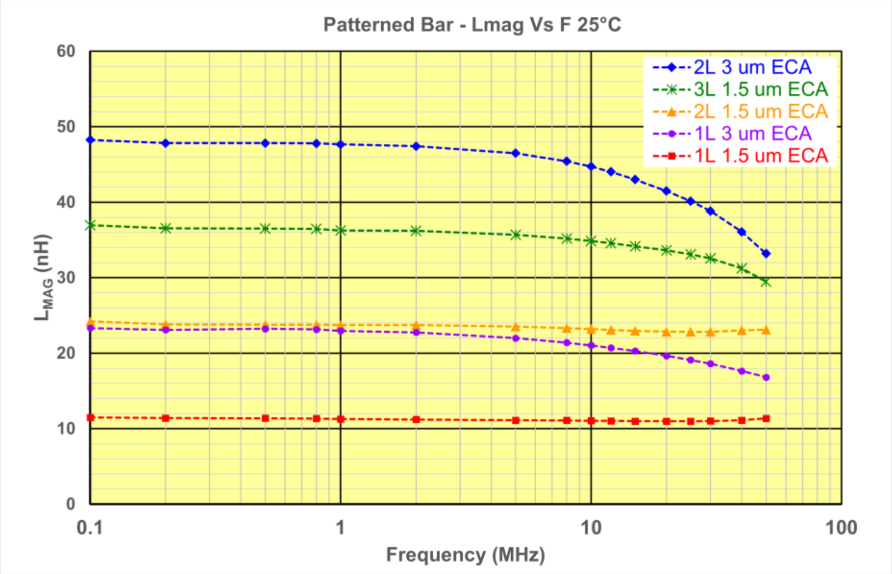


Higher values of $B_{USEABLE}$ support higher value of $B_{DC} + \Delta B/2$
Higher values of $\Delta B/2$ enable higher volt-second stress
Higher volt-second stress enables higher input voltage buses beyond 12V towards 18V/24V

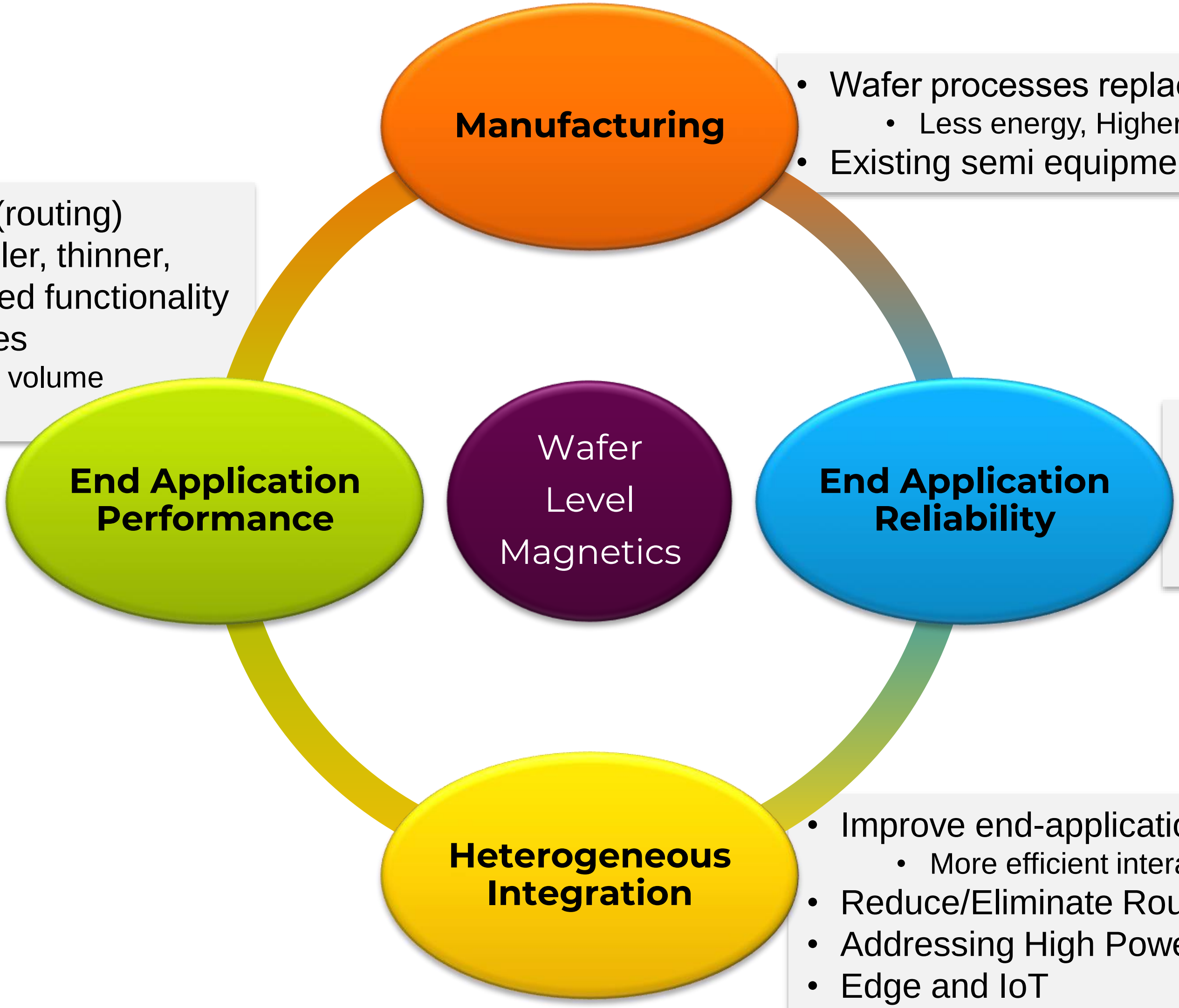
L_{F_MAG} Vs F (100 kHz – 50 MHz)
Scalability By Layers and Thickness







Wafer Level Magnetics
(Impacts on Environmental Sustainability)



Wafer Level Magnetics

Manufacturing

- Wafer processes replace “dirty” discrete manufacturing
    - Less energy, Higher Yield Processes
- Existing semi equipment across devices/components

End Application Performance

- Reduce energy transfer loss (routing)
- Integrated magnetics → smaller, thinner, more efficient devices → added functionality
- Tighter specification tolerances
    - Better utilization of physical volume
    - Tighter design margins

End Application Reliability

- Lower failure rates – less waste
- Reduced replacement cost
- Reduced downtime costs due to system failures

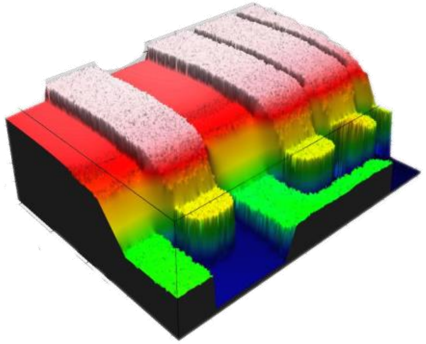
Heterogeneous Integration

- Improve end-application performance
    - More efficient interaction between devices on common substrate
- Reduce/Eliminate Routing
- Addressing High Power Compute
- Edge and IoT

Device Examples

- Thick Cu toroid micro-inductors
- Multi-core toroids
- Spiral coils
- Electromagnets/Actuators
- Transformers
- Sensors

Inductance density:	100nH/mm^2
	2nH/mΩ
Power Throughput:	0.5W ≤ P ≤ 15W
Current range:	0.5A ≤ I ≤ 5A
Operational V_{IN}:	1.8 V_{DC} ≤ V_{IN} ≤ 18 V_{DC}
Operational V_{OUT}:	0.6 V_{DC} ≤ V_{OUT} ≤ 5 V_{DC}
Working Voltage:	50 V_{DC}
Frequency Range:	5 MHz ≤ f ≤ 30 MHz
Typical Thickness:	40 um ≥ T ≤ 200 um

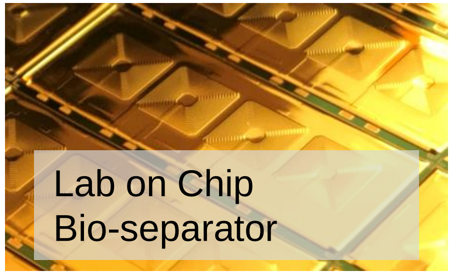


3D topography

10MHz Isolator Transformer

High current thin film inductor

2A spiral inductor



Lab on Chip Bio-separator

Walk away message:

Continuous electroplating of magnetic film and insulator sequentially is a viable technology that **has been demonstrated** at the wafer level

That enables:

Single mask thin film magnetic core laminations for high performance wafer level magnetics that support heterogeneous integration

Fast, Low cost, environmentally friendly BEOL – CMOS/GaN compatible simple manufacturing process with existing infrastructure

Wafer level magnetics enables heterogenous integration improving:

system technical performance
manufacturing and assembly sustainability performance

Thank you!