# Class I Multi-Layer Ceramic Capacitors (MLCCs) Performance as Wide Band Gap (WBG) Snubbers in Hard Switching Applications

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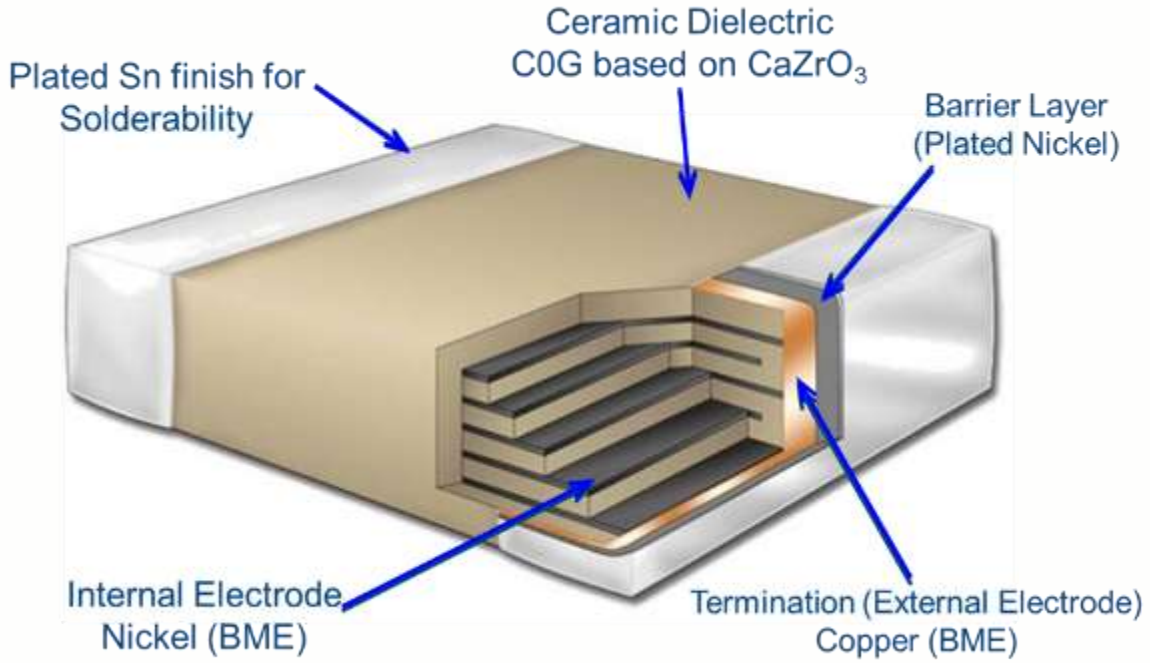
# Study Background

- Previous high dV/dt MLCC testing was limited to 30V/ns and 500V using silicon mosfets.
- In this work the internal charging current stresses induced by higher dV/dt pulses in low capacitance, high voltage rated MLCCs (> 500 VDC) used as snubbers in Wide Band Gap(WBG) device switching cells was studied.
- Packaging snubber capacitors close to WBG device improves performance, ultimately being most effective packaged inside power modules.  MLCCs were tested with high dV/dt stress at 150 C to replicate power module conditions as well.

# Base Metal Electrode (BME) MLCC Construction




**C** = Design Capacitance

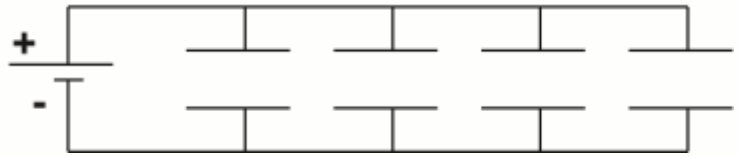
**K** = Dielectric Constant

**A** = Overlap Area

**d** = Ceramic Thickness

**n** = Number of Electrodes

$$C = \frac{e_0 K A (n-1)}{d}$$



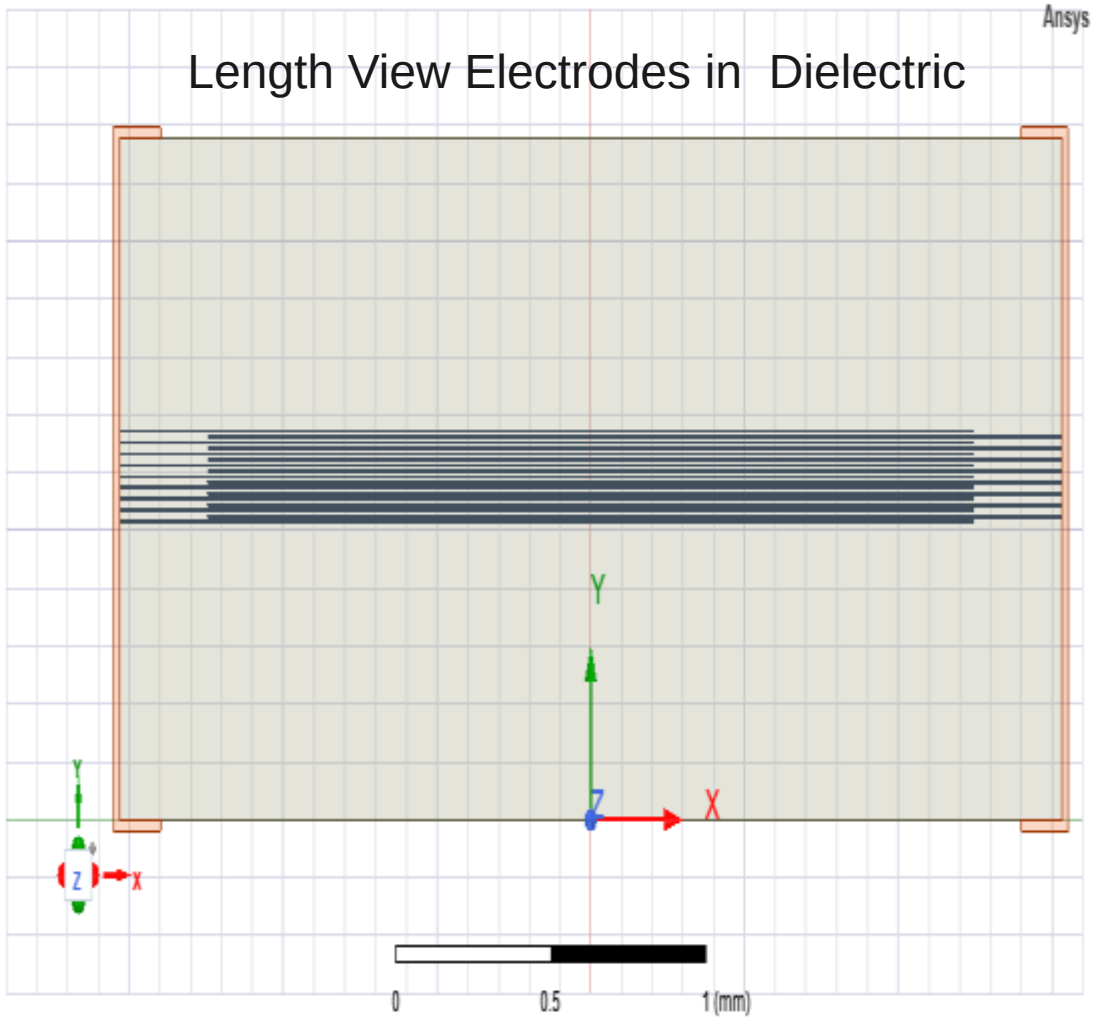

$$C_T = C_1 + C_2 + C_3 + \ldots C_n$$

Voltage rating depends on Ceramic dielectric thickness (breakdown E field strength )
Thicker dielectrics, wider plate separation are required for higher voltage capacitors.

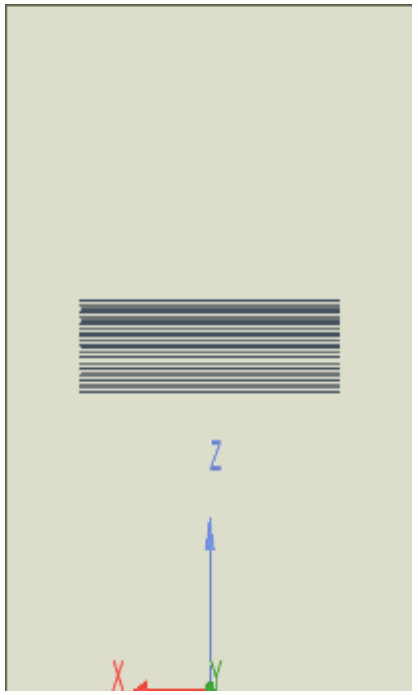
# Internal Construction

## C0G 1206 470pF 630V Standard Electrode (C1206C471JBGAC)

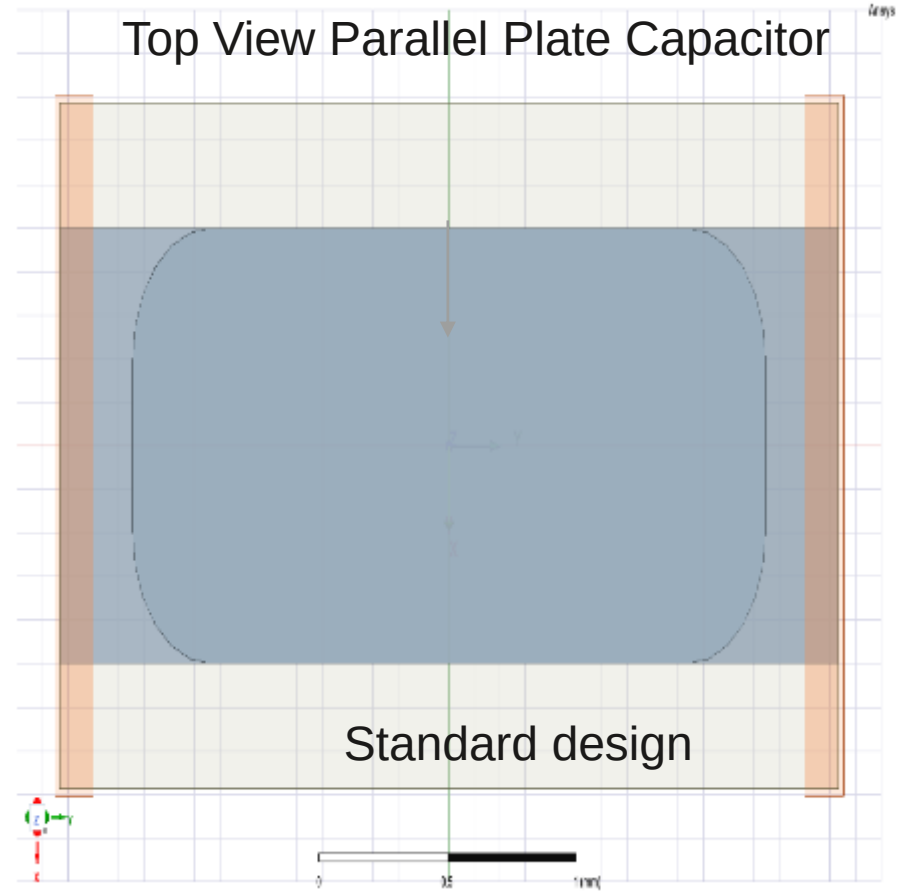
Length View Electrodes in Dielectric




End Termination View




Top View Parallel Plate Capacitor



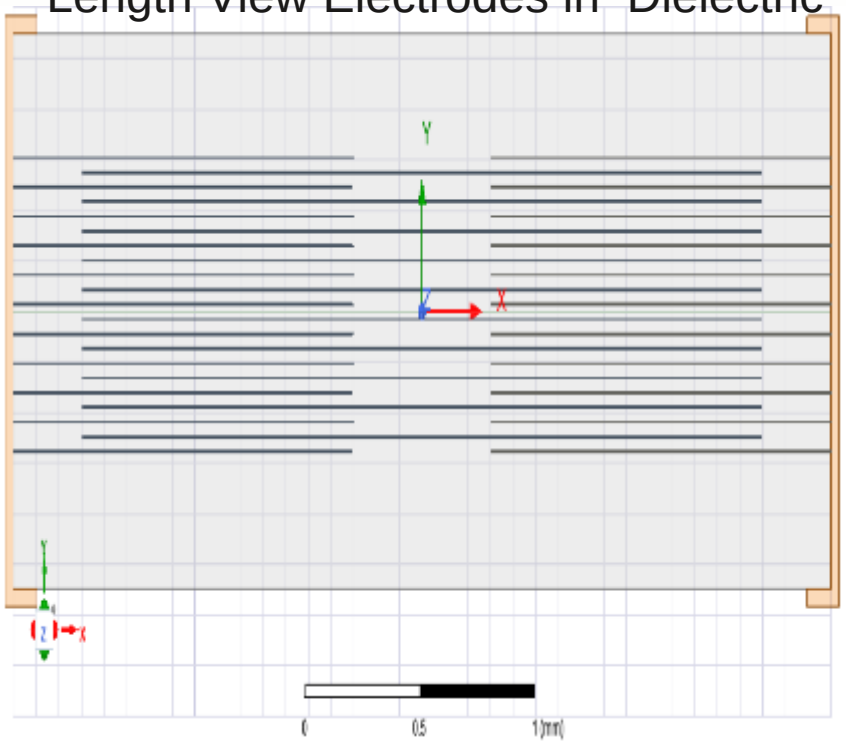

1 Active ( parallel plate capacitor overlap) sees full dV/dt across terminals

# Internal Construction

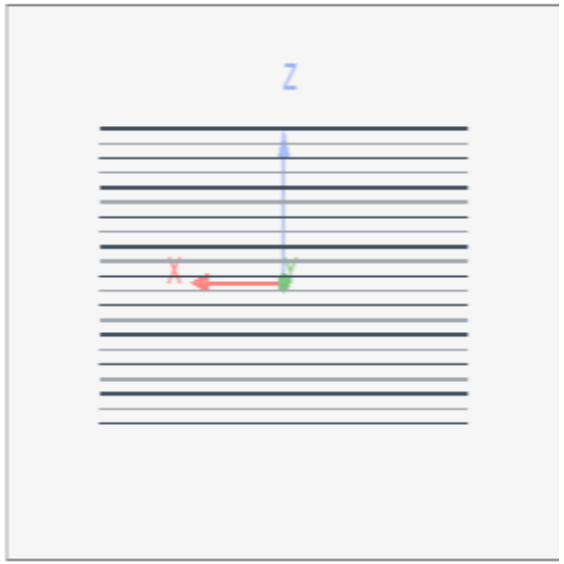
C0G 1206 100pF 2000V 2-Serial Electrode (C1206H101JGGAC)
C0G 1206 68pF 2000V 2-Serial Electrode (C1206H680KGGAC)

Thicker dielectric, smaller plate area

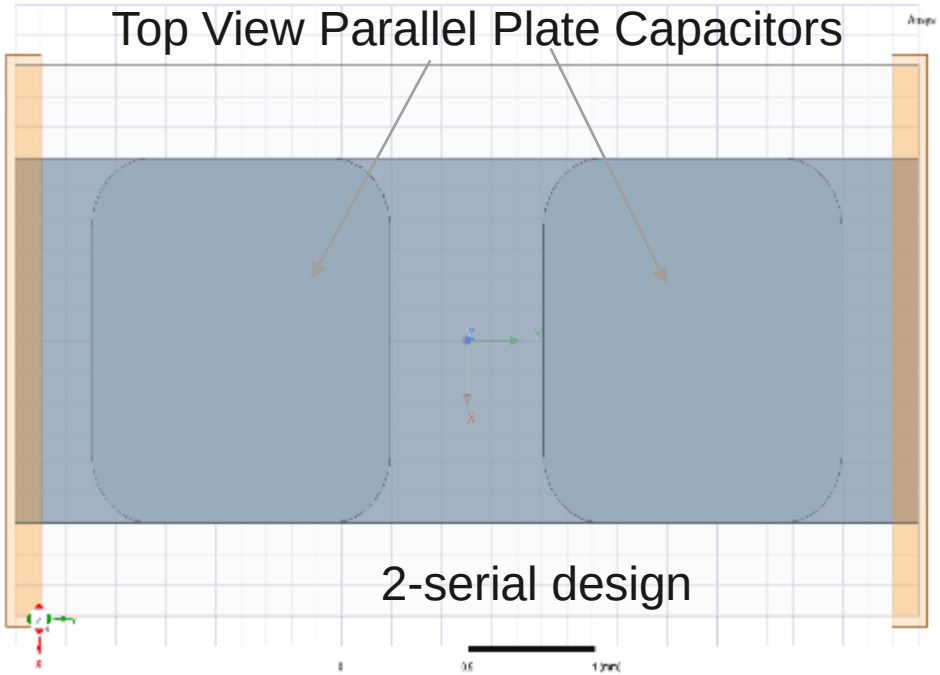
Length View Electrodes in Dielectric



End Termination View



Top View Parallel Plate Capacitors

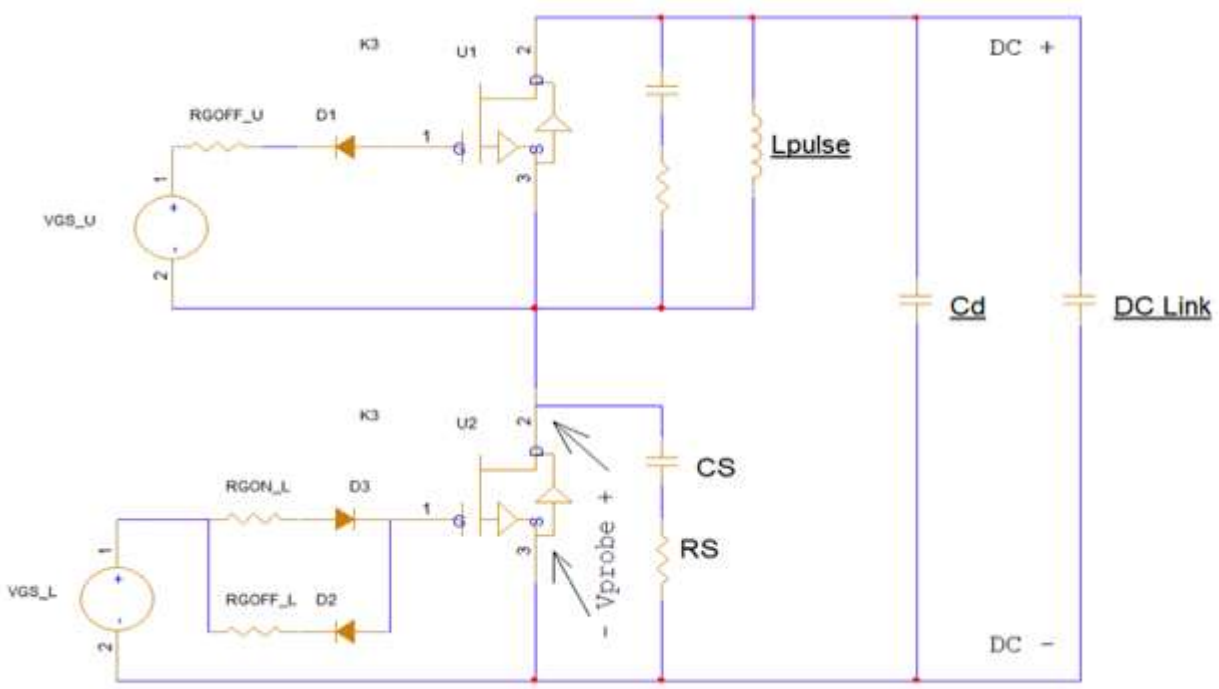


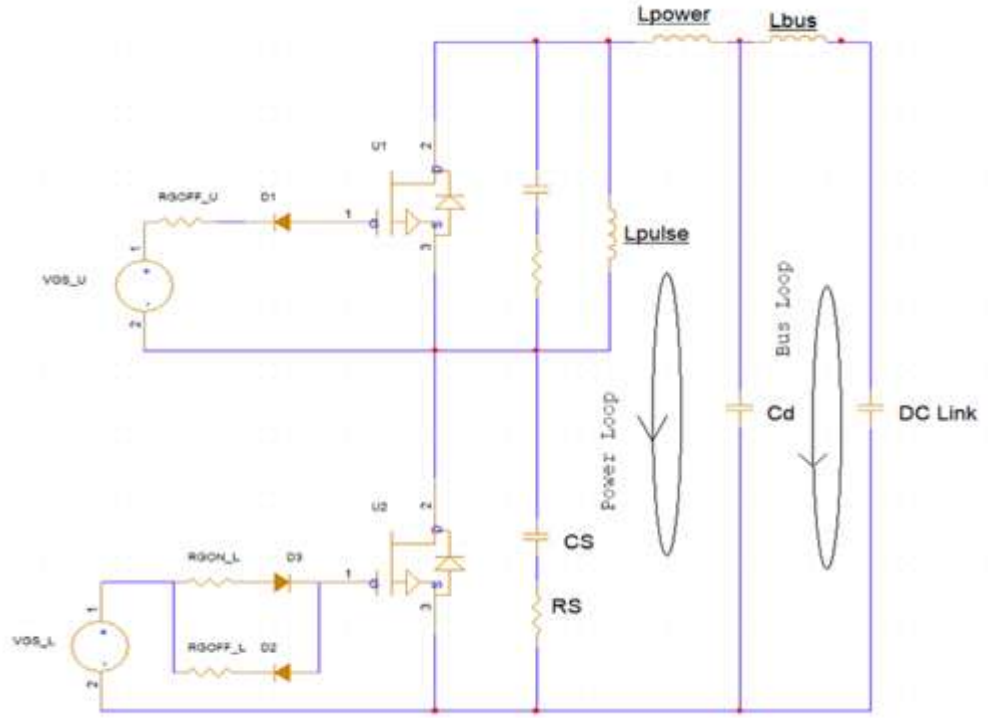
2-serial design

Two Actives in series each see ½ of the dV/dt across terminals

# Experimental Inductive Double Pulse Test Setup

Power Loop Lumped Inductance L power and WBG Switch Coss  resonate




Mike Zhu, “Switching Fast SiC FETs with a Snubber” UnitedSiC_AN0018 Application Note – November 2018. www. Unitedsic.com

# Measured Results

Double pulse waveform probed across drain to source of a  UnitedSiC prototype 2 kV/60 mΩ discrete SiC FET switching 1200 V, 25 A with no snubber

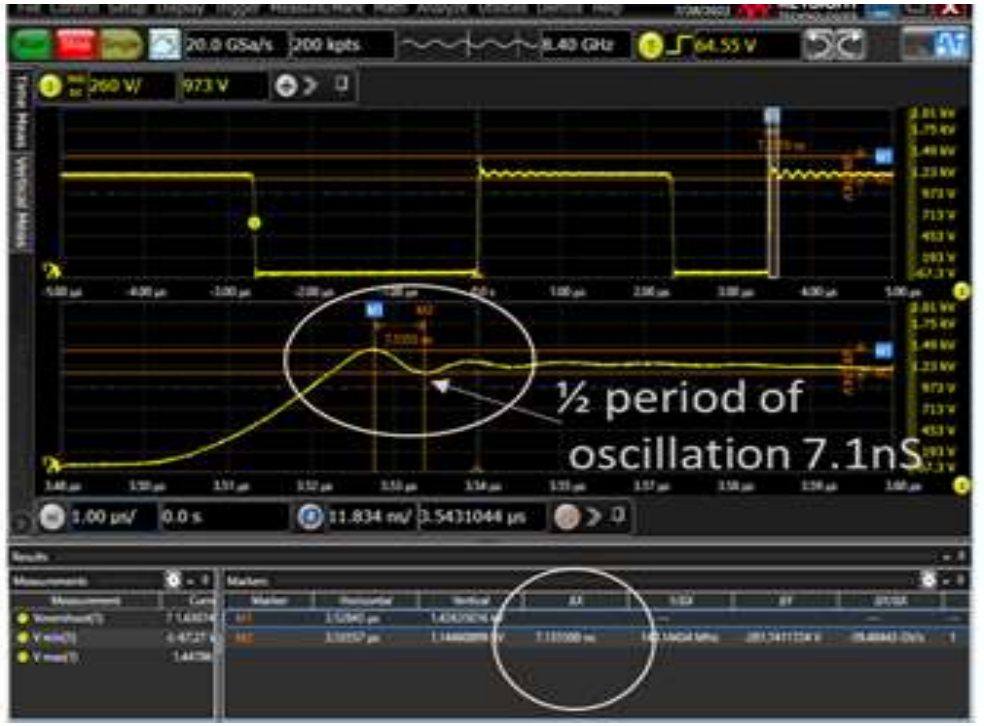


dV/dt of 70 V/ns, $V_{overshoot}$ of 1.47 kV, and loop resonant frequency of approximately 580 MHz.

# Measured Results

2 kV/60 mΩ discrete FET switching 1200 V, 25 A; C1206H101JGGAC 100pF 2000V snubber capacitor with dV/dt of 52 V/ns, Vovershoot of 1.43 kV, oscillation frequency of approximately 440 MHz at a pulse repetition rate of 120 Hz.

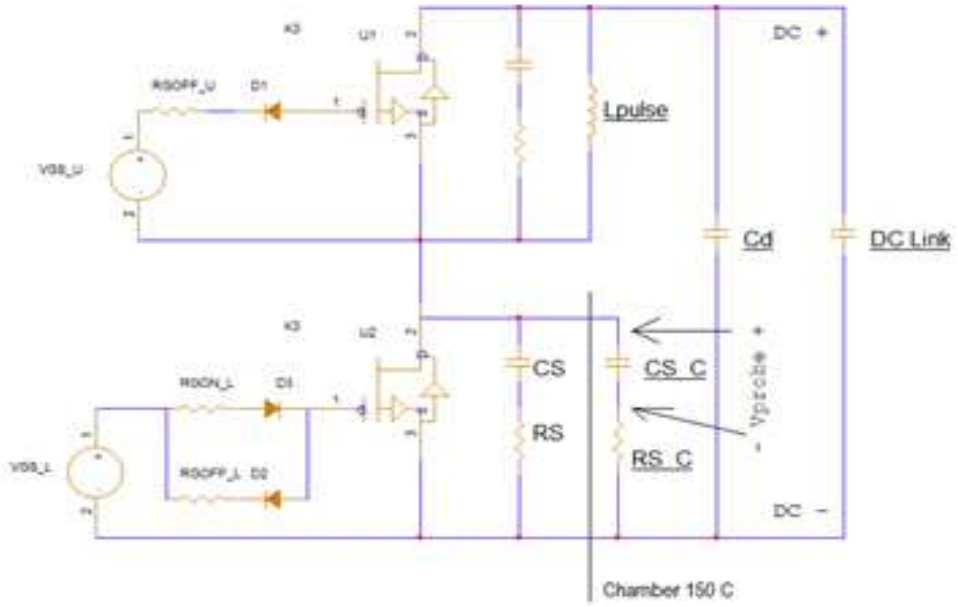
Recommended snubber cap value Cs is 100pF ~ 3 X FET Coss value (35pF ) in series Rs value of 5 Ω


No degradation in Cap DF or IR to catalog limits after 10 million pulses for 5 samples
UnitedSiC SiC FET User Guide" Feb 2020, https://unitedsic.com/guides

# Measured Results

UF3C120040K4S switching 800V 50A ~ 140pF total snubber capacitance.
Two series RC snubbers using a C1206H680KGGAC7800 68pF 2000V 200°C in series with 10 Ω Rs one on double pulse board and a second on a separate test board across output inside Chamber. A slow 10 Hz pulse repetition rate was used



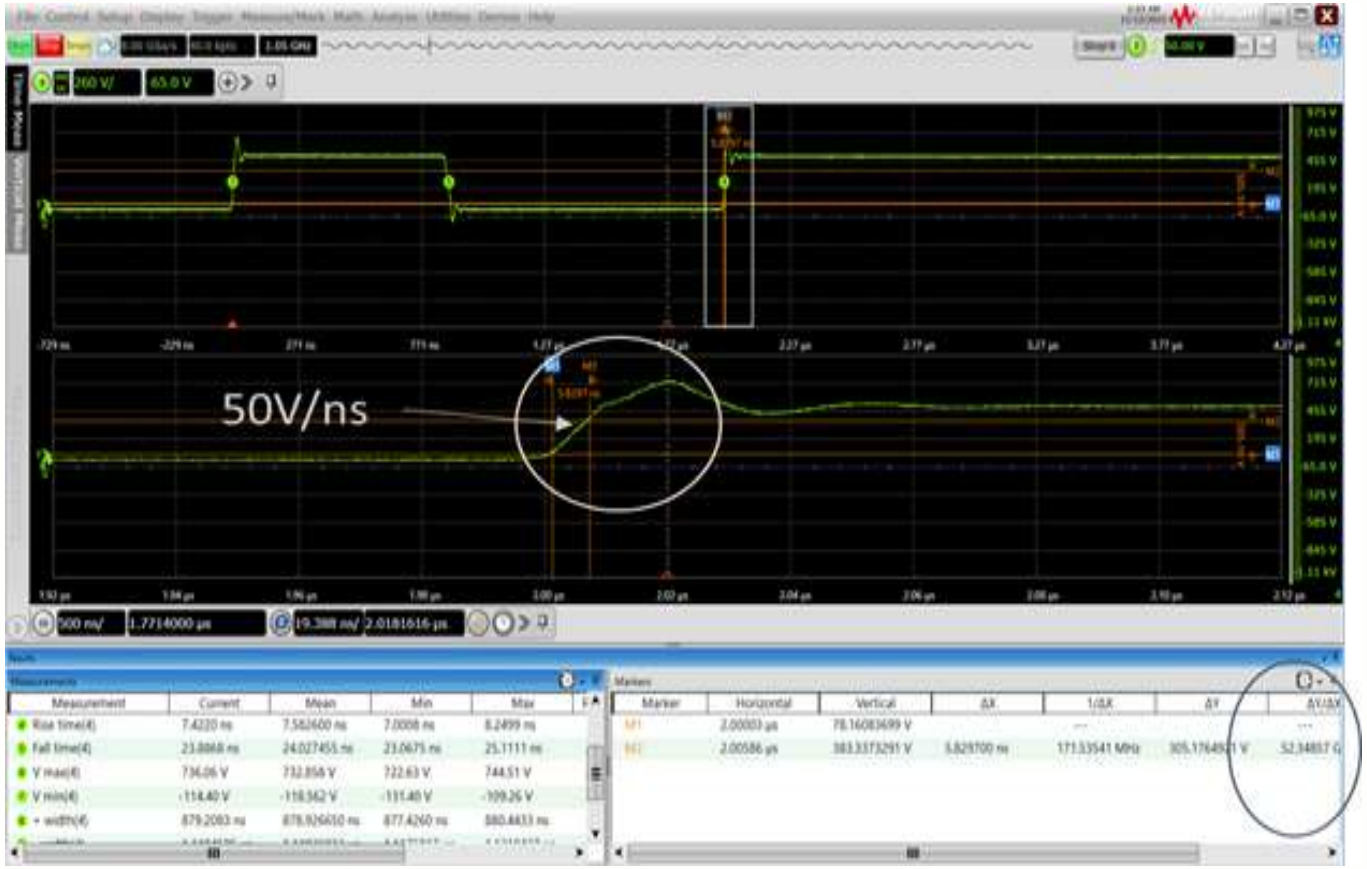


dV/dt across MLCC in chamber at 25 C measured with differential probe ~ 50V/ns .

No degradation in Cap DF or IR to catalog limits after 500 thousand pulses at 150° C for 5 samples

# Measured Results

UF3C120040K4S switching 500 V 50 A with C1206C471JBGAC and Rs 3.3 Ω  dV/dt is approximately 50 V/ns at 120 Hz pulse repetition rate




No degradation observed in Cap DF or IR  to catalog limits after 10 million pulses for 5 samples

# Charging Current Density Calculation

$$\text{Charge } (Q_{active}) = C_{active} \cdot V$$

$$(dQ_{active})/dt = C_{active} \cdot dV/dt$$

$$\text{Current } (I_{active}) \sim C_{active} \cdot dV/dt$$

$$I_{electrode} \sim 2 \cdot I_{active}$$

$$\text{Current Density } (J_{electrode}) = 2^* C_{active}^*(dV/dt) /(W \cdot th)$$

where W is the electrode width ~ 1mm and th is the electrode thickness ~ 1.5 um.

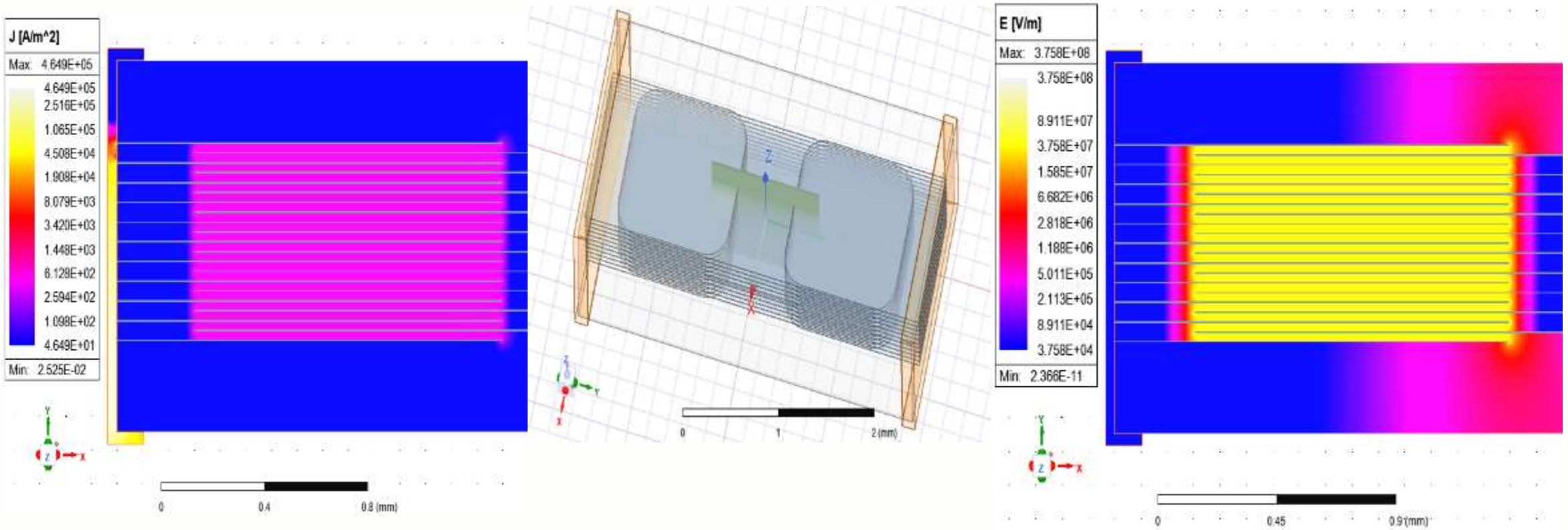
Cross-sectional Area of 1.5E-3 $mm^2$

| Design | Cap Per Active | dV/dt | Charge (Q) per Active | Current (I) Per Electrode | Current Density (J) Per Electrode |
|---|---|---|---|---|---|
| | pF | V/ns | Coulomb | A | $A/mm^2$ |
| **C1206H101JGGAC** | 10 | 25 | 2.5E-10 | 0.5 | 330 |
| **C1206C471JBGAC** | 30 | 50 | 1.5E-9 | 3.0 | 2000 |

No degradation in Cap DF or IR to catalog limits

# ANSYS® Maxwell® 3D Simulation

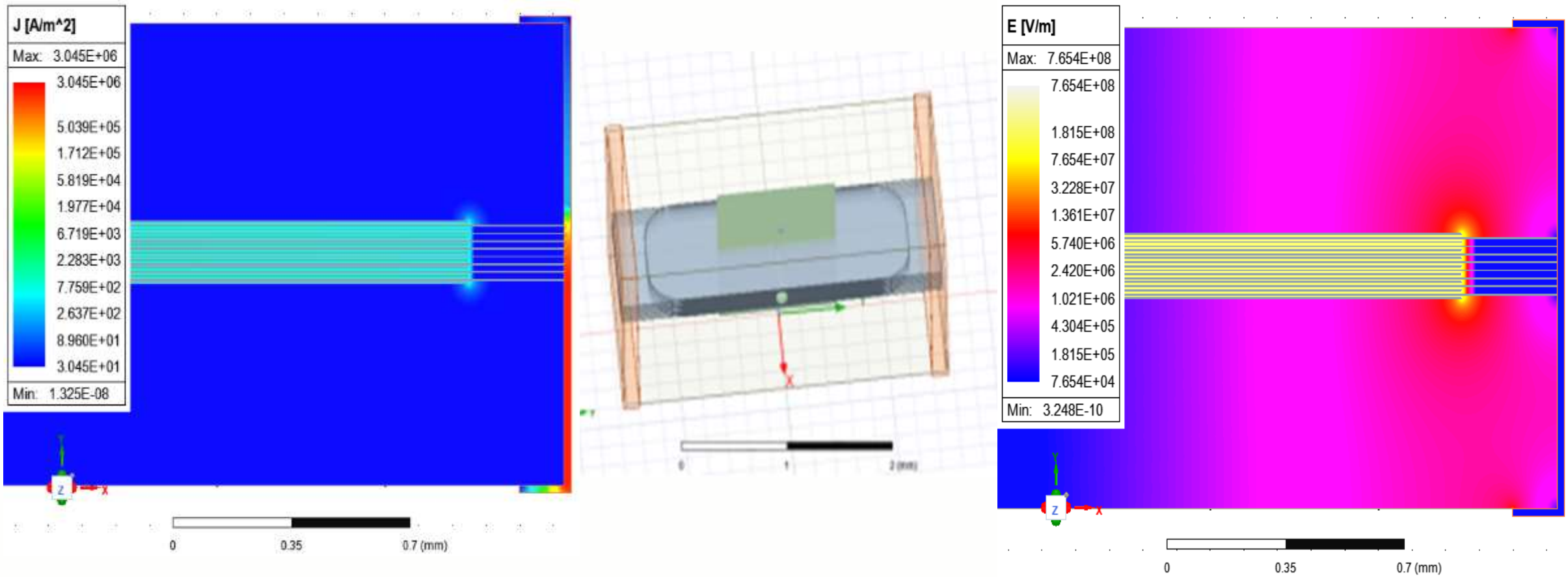
C1206H101JGGAC conduction current density, JC, in termination and electrodes and displacement current density, JD, in dielectric at 90 MHz 270 V peak to peak oscillation condition. Maximum electric field in dielectric at end of the electrodes at peak overshoot voltage 1500V




ANSYS® Maxwell® 3D Model Cut plane in center for 2D current density and electric field plots

# ANSYS® Maxwell® 3D Simulation

C1206C471JBGAC conduction current density, JC, in terminations and electrodes and displacement current density, JD, in dielectric at 33MHz 260 V peak to peak oscillation condition . Maximum Electric Field in dielectric at end of the electrodes at peak voltage 630 V




ANSYS® Maxwell® 3D Model Cut plane in center for 2D current density and electric field plots

# Conclusions

- The experimental results show both the 2-serial and standard designs are not degraded by high dV/dt switching transients.
- The higher voltage 2-serial electrode designs with lower cap per active, have lower transient current density and lower electric field stress from modeling.
- These low capacitance, high-voltage and high-temperature capable C0G MLCCs can be effectively integrated as snubbers in WBG power modules.

# Acknowledgements


- KEMET Electronics would like to thank the team at UnitedSiC (Qorvo) for their support in this effort.