3D-PEIM 2026 Program

Day 1 - Monday November 16, 2026

Time	Description/Title	Presenter	Affiliation
12:00	Registration Opens		
	Tutorials 1 & 2		
13:00 - 15:00	State of the Art in Semiconductor Packaging Technologies	Chris Bailey Hongbin Yu Chanyeop Park George Dogiamis	ASU DECA
	Trends in Magnetic Material Properties	Matt Wilkowski	Wurth Elektronik
15:00 - 15:15	Coffee Break		
	Tutorials 3 & 4		
15:15 - 17:15	TBD	TBD	Indium Corporation
	Digital Twin for Electronics Packaging	Jong Ryu	NC State Univ
17:15 - 17:30	Coffee Break		
	Panel Session		
17:30 - 19:00	Key Challenges for 3D Power Electronics Packaging & Manufacturing	Chris Bailey Doug Hopkins Pat McCluskey George Dogiamis Francesco Carobolante Ravi Mahajan	ASU NC State Univ Univ of Maryland DECA IoTissimo Intel

Day 2 - Tuesday November 17, 2026

Time	Description/Title	Presenter	Affiliation
7:30	Registration Opens		
7:30 - 8:30	Continental Breakfast		
8:30 - 8:45	**General Chair Welcome**	Chris Bailey	ASU
8:45 - 9:30	Plenary 1: Rethinking Power Delivery for Next Generation AI Accelerators (Session Chair: Chanyeop Park)	Kaladhar Radhakrishnan	Intel
	Session 1: Advanced Packaging & 3D Integrated Modules		
	Co-Chairs	Raja Ayyanar	ASU
		Hongbin Yu	ASU
9:30 - 10:00	Keynote: 3D-Integrated Vertical Power Delivery: Achieving >100% Perf/W Gains in Multi-Kw Chiplet Stacks	Francesco Carobolante	IoTissimo
10:00 - 10:15	Break		

Day 2 - Tuesday November 17, 2026 cont'd

Time	Description/Title	Presenter	Affiliation
10:15 - 10:40	Emerging Hi Developments for Power Electronics	Jason Neely	Sandia National Laboratories
10:40 - 11:05	Power Electronics Re-Invented: AI as Key Enabler for Power Device Innovation	Peter Kanschat	Infineon
11:05 -11:30	Scalable and Miniaturized 3D Peek Package for High-Power Density and High-Efficiency DC-DC Converters for High-Performance Computing	Tim Nils Bierwirth	Leibniz Univ Hannover
11:30 - 13:00	Partner Exhibits and Lunch		
13:00 - 13:45	Plenary 2: Scaling Vertical Power Delivery for AI Computing: a PPACt-Driven Materials and Process Perspective (Session Chair: Chanyeop Park)	Yi Zheng	Applied Materials
	Session 2: Materials for Advanced Packaging		
	Co-Chairs	Chanyeop Park	ASU
		Adam Morgan	NoMIS Power
13:45 - 14:15	Keynote: Material-Driven Electric Field Engineering for Reliable High-Voltage Power Modules: Field Grading Materials and Nanocomposite Dielectrics	Muneaki Kurimoto	Nagoya Univ
14:15 - 14:40	Integrated Magnetic Cores: Needs and Unknowns	Alex Hanson	UT-Austin
14:40 - 15:05	Microsized Silver–Aluminum Sintering Paste with Enhanced Joint Reliability for SiC Power Modules	Ryoma Tokonami	Univ of Osaka
15:05 - 15:30	Effect of a Polymer Nanocomposite on Surface Flashover in Power Converters at High Elevation	Peiyuan Sun	Virginia Tech
15:30 - 16:00	Partner Exhibits and Break		
	Session 3: Thermal Management		
	Co-Chairs	Jong Ryu	NC State Univ
		Robert Wang	ASU
16:00 - 16:30	Keynote: Phased Array with Innovative Heterogeneously Integrated Thermal Solution	Christopher Roper	HRL
16:30 - 16:55	Current Challenges and Developments in Single- and Two-Phase Liquid Cooling	Dave Saums	DS&A LLC
16:55 - 17:20	Implementing a Solder Thermal Interface Material (sTIM) for Cost-Performance Balance in Molded Power Module to Heat Sink Attach	Ryan Mayberry	Indium Corporation
17:20 - 17:45	Defect-Aware Thermal Bottleneck Analysis in SiC/Si Heterogeneous Stacks for Advanced Packaging	Md Rifat E Rasul	ASU
17:45 - 19:00	Poster Presentations and Welcome Reception		

Day 3 - Wednesday November 18, 2026			
Time	**Description/Title**	**Presenter**	**Affiliation**
7:30	Registration Opens		
7:30 - 8:30	Continental Breakfast		
8:30 - 9:15	Plenary 3: Heterogeneous Integration of Vertical Power Delivery for AI and High Performance Computing (Session Chair: Chanyeop Park)	Cian O'Mathuna	Tyndall National Institute
	Session 4: Design, Modelling, & Simulation		
	Co-Chairs	Doug Hopkins	NC State Univ
		Leslie Hwang	ASU
9:15 - 9:45	Keynote: Toward AI-Driven Power Electronics Co-Design: Physics-Informed Learning, Topology Generation, and Packaging Optimization	Leslie Hwang	ASU
9:45 - 10:10	Handling the Design Complexity in Power Electronics Possessing Heterogeneous Functionality with AI-enabled EDA Tools	John Damoulakis	Cadence
10:10 - 10:25	Break		
10:25 - 10:50	A Heterogeneously Integrated Fan-Out Wafer-Level Package Architecture for GaN-on-SiC Power Amplifiers: Electro-Thermal and Thermo-Mechanical Evaluation	Pallavi Jithendrriyan	ASU
10:50 - 11:15	From Chip to Chiller: System-Level Impact of Power Delivery Architecture on Data Center Cooling Costs	Ben Schuchardt	Purdue Univ
11:15 - 12:00	**Exhibitor Presentations**		
12:00 - 13:30	Partner Exhibits and Lunch		
13:30 - 14:15	Plenary 4: Integrated Vertical Power Delivery for AI Datacenters – Challenges & Opportunities (Session Chair: Chanyeop Park)	Madhavan Swaminathan	Penn State Univ
	Session 5: Reliability & Failure Analysis		
	Co-Chairs	Jeff Ewanchuk	RTRC
		Brian Narveson	PSMA
14:15 - 14:45	Keynote: Liquid-Metal Interconnects for Power Semiconductors	Nick Baker	Univ of Alabama
14:45 - 15:10	Thermomechanical Reliability of Space Power Advanced Module	Pat McCluskey	Univ of Maryland
15:10 - 15:35	Real-Time In-Situ Dual-Pulse Testing of Switching Characteristics in Phase-Shift Full-Bridge Converters via Backward Operation	Sooan Pack	Univ of Rhode Island
15:35 - 16:00	Parameterized PINNs for Warpage Prediction in Heterogeneous Multi-Chip Module Packages	Alec Bunn	ASU
16:00 - 16:30	Partner Exhibits and Break		

Day 3 - Wednesday November 18, 2026 cont'd

Time	Description/Title	Presenter	Affiliation
	Session 6: Passive Components		
	Co-Chairs	Trifon Liakopoulos	Eneira
		Kousuke Miyaji	Shinshu Univ
16:30 - 17:00	Keynote: Silicon Capacitor Array chiplet for Power Design Network with a Wide Voltage Range	Jerry Zhai	Max Epic
17:00 - 17:25	Improving Current Density in Vertical power Delivery (VPD) multiphase Coupled Inductors	Allen Nguyen	Dartmouth College
17:25 - 17:50	Overcoming the Magnetics Bottleneck in Vertical Power Delivery for AI	Youssef Elasser	NVIDIA
17:50 - 18:15	Breaking the “Current” Barrier: Electroplated Integrated Magnetics for 3D-Hi Vertical Power Delivery	Kamyar Ahmadi	Eneira
19:00 - 22:00	Gala Dinner (Buses depart to the Desert Botanical Garden at 18:30)		

Day 4 - Thursday November 19, 2026

Time	Description/Title	Presenter	Affiliation
7:30	Registration Opens		
7:30 - 8:45	Continental Breakfast		
8:45 - 9:30	Plenary 5: 3D 3D Panel Level Packaging and Advanced Compact 3D Module Architectures for AI Data Center Power Electronics (Session Chair: Chanyeop Park)	Stephen Coates	Yuxuan Semiconductor Consulting Company
9:30 - 10:15	Plenary 6: AI Trajectory and its Demands on Power Delivery (Session Chair: Chanyeop Park)	Rinkle Jain	NVIDIA
10:15 - 10:30	Break		
	Session 7: Power Delivery & Energy Storage		
	Co-Chairs	Francesco Carobolante	IoTissimo
		Yi Zheng	Applied Materials
10:30 - 11:00	Keynote: Power Delivery as the definitive frontier of AI Performance	Ahmed Abou-Alfotouh	AMD
11:00 - 11:25	Passives Technology for Vertical Power Delivery Architectures for AI and HPC PDN Solutions	Bart Deprospo	Saras Micro Devices
11:25 - 11:50	Powering the AI Era: High-Density Integrated Voltage Regulators	Noah Sturcken	Ferric
11:50 - 13:00	Box Lunch		
13:00 - 17:00	**Lab Tour**		